UNIVERSIDADE DE SANTIAGO DE COMPOSTELA

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PhD THESIS

MODELLING AND CHARACTERIZATION OF SMALL PHOTOSENSORS IN ADVANCED CMOS TECHNOLOGIES

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HEREBY CERTIFIES:

That the dissertation entitled **Modelling and characterization of small photosensors in advanced CMOS technologies** has been developed by **Mrs. Beatriz Blanco Filgueira** under my direction at the Department of Electronics and Computer Science of the University of Santiago de Compostela in fulfillment of the requirements for the Degree of Doctor of Philosophy.

Santiago de Compostela, July 2012

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HACE CONSTAR:

Que la memoria titulada **Modelling and characterization of small photosensors in advanced CMOS technologies** ha sido realizada por **Dña. Beatriz Blanco Filgueira** bajo mi dirección en el Departamento de Electrónica y Computación de la Universidad de Santiago de Compostela, y constituye la Tesis que presenta para optar al título de Doctor por la Universidad de Santiago de Compostela.

Santiago de Compostela, julio de 2012

Paula López Martínez
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Beatriz Blanco Filgueira
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A Juan, Guille, Amparo e Carlos,
o meu fogar.

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Máis alá do ámbito profesional, as nosas vidas están cheas de persoas que dunha maneira ou doutra inflúen positivamente en todo o que facemos. Persoas coas que compartimos risas, que celebran os nosos logros, que nos levantan cada vez que caemos, coas que podemos contar sempre. Máis alá de agradecerlle dende aquí todo o que levan aportado á miña vida, espero agradecerllo cos meus actos, día a día, e estar á altura do que se merecen. Vós sodes o verdadeiramente importante.

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Resumen

Siguiendo el reglamento de los estudios de tercer ciclo de la Universidad de Santiago de Compostela, aprobado en la Junta de Gobierno el día 7 de abril de 2000 (DOG de 6 de marzo de 2001) y modificado por la Junta de Gobierno de 14 de noviembre de 2000, el Consejo de Gobierno de 22 de noviembre de 2003, de 18 de julio de 2005 (artículo 30 a 45), de 11 de noviembre de 2008 y de 14 de mayo de 2009; y, concretamente, cumpliendo las especificaciones indicadas en el capítulo 4, artículo 30, apartado 3 de dicho reglamento, se muestra a continuación un resumen en castellano de la tesis.

El mercado de los sensores de imagen, y en concreto el de las cámaras digitales, continúa dominado por un constante aumento del número de píxeles. Para ello, las tecnologías de sensores de imagen predominantes en la actualidad, CMOS (*Complementary Metal-Oxide Semiconductor*) y CCD (*Charge Coupled Devices*), compiten tanto por los segmentos de mercado existentes como por los emergentes adaptándose a esta tendencia de forma que los dispositivos sigan ofreciendo un buen rendimiento en términos de coste, consumo y peso, entre otros. Los beneficios potenciales de los sistemas de imagen CMOS ya fueron pronosticados a finales de los años 90 [1], y solo algunos años más tarde demostraron un rendimiento competitivo en comparación con los CCDs, [2]. Entre las ventajas de los sensores de imagen CMOS, tales como la reducción del consumo de energía y del coste, tal vez la miniaturización y la funcionalidad *on-chip* sean las que se ven más favorecidas por el escalado de la tecnología CMOS [3]. El principal camino para alcanzar tamaños de píxel cada vez más pequeños y, por tanto, mayor resolución con el mismo área, pasa por utilizar nodos tecnológicos avanzados. Pero, a pesar de que el progreso en la tecnología CMOS ofrece los medios para fabricar píxeles cada vez más pequeños, éstos deben superar algunos problemas electrónicos y ópticos inherentes a estas tecnologías. De hecho, aunque algunos estudios eran optimistas sobre los

beneficios de los sistemas de imagen CMOS a finales de los años 90, también se cuestionaba su calidad más allá del nodo tecnológico de 0.25 μm, si no se realizaba ningún cambio en el proceso, debido al aumento de la corriente de fuga y a la disminución del rango dinámico debido a los efectos del escalado [4]. Hoy en día, muchos de estos problemas se han minimizado gracias a los avances en la ingeniería de procesos, pero el desafío de producir el píxel más pequeño posible con la suficiente sensitividad sigue existiendo. Por otro lado, los componentes fotónico-electrónicos integrados siguen estando dominados por la característica de la reducción de tamaño en las tecnologías CMOS, conocida como Ley de Moore [5]. Debido a que los sistemas de imagen deben interactuar con la luz, el impacto de la Ley de Moore sobre ellos es diferente al que tiene lugar sobre otras aplicaciones de circuitos integrados. De este modo, también debe investigarse cómo la tendencia a la reducción del tamaño de los píxeles interactúa con las propiedades de la luz, tales como el ruido fotónico y la difracción.

El mercado de los sensores de imagen CMOS ha aumentado considerablemente en los últimos años favorecido por los avances en la tecnología de fabricación. Paralelamente a todo esto, ha habido una gran preocupación en relación con el impacto del escalado de la tecnología y el dispositivo en la respuesta global [4], en particular en términos de sensitividad [6], corriente oscura [7] y respuesta espectral [8]. Sin embargo, el estudio de los efectos dimensionales sobre los sensores CMOS cada vez más pequeños es esencial dado que su modelado y simulación representan un punto débil en el diseño de nanosensores de imagen. Esta deficiencia debe ser abordada, ya que constituye una de las pocas metodologías que permiten reducir los tiempos y costes de desarrollo. Por lo tanto, es necesario un esfuerzo con un enfoque que combine el proceso tecnológico, la arquitectura del píxel y el modelado de los sensores CMOS para alcanzar el rendimiento de los CCDs a medida que se reduce el tamaño del píxel [9].

En los últimos años, los esfuerzos para modificar los procesos de fabricación de las tecnologías CMOS estándar y así mejorar el rendimiento de la formación de imágenes, han sido significativos, [10]. Para mejorar la fotoresponsividad, se han incluido diodos de unión profunda sin siliciuros con perfiles optimizados de dopaje en los procesos estándar. Por otro lado, la reducción de la corriente oscura se consigue por medio de la implantación de difusiones dobles de fuente/drenador sin siliciuros así como de estructuras de diodo *pinned*. El recocido por hidrógeno se utiliza también para reducir las fugas debidas a defectos por pasivación. La reducción de fugas en los transistores, tanto en el de *reset* como en el seguidor en un sensor de píxel activo, también se ha considerado a través del uso de óxido de puerta grueso. Además, se aumenta la tensión umbral del transistor de reset y se disminuye la del seguidor para reducir

su corriente de apagado y para mejorar la oscilación de voltaje, respectivamente. Finalmente, en tecnologías de sensores de imagen (CIS) y después de la pasivación, se pueden depositar sobre el chip un filtro de color y microlentes para mejorar la eficiencia cuántica.

Por otro lado, el escalado de la tecnología también tiene efectos perjudiciales sobre la eficiencia óptica del píxel que han sido igualmente abordados por las mejoras tecnológicas [11]. Por ejemplo, la transmisión de la luz se ve reducida por el uso de dióxido/nitruro de silicio. Además, a medida que la tecnología CMOS escala, la distancia desde la superficie del chip al fotodetector aumenta en relación con el tamaño del pixel más pequeño que se puede fabricar. Esto es debido a una reducción más lenta en el espesor de las capas de interconexión, que escala menos que en las otras dos dimensiones. Como resultado, la luz debe viajar a través de un túnel cada vez más profundo y más estrecho antes de llegar a la superficie del fotodetector. Por otro lado, también se están utilizando óxidos con mejores propiedades para la transmisión de la luz con el propósito de aumentar la eficiencia óptica. Además, el adelgazamiento de las capas de metal y óxido se utiliza para disminuir la relación de aspecto del túnel por encima de cada fotodetector, [12]. Otra técnica para aumentar la eficiencia óptica es la colocación de burbujas de aire alrededor de cada píxel con el fin de crear una guía de onda óptica rudimentaria mediante la cual la luz incidente en la superficie es guiada hasta el píxel correspondiente a través de la reflexión interna total. Las burbujas de aire también sirven para reducir significativamente la contaminación espacial óptica, que puede ser particularmente problemática a medida que el tamaño del píxel disminuye, [13]. Todas estas modificaciones a nivel de proceso han permitido la reducción del tamaño del píxel por debajo de los valores pronosticados.

En cuanto a la arquitectura del píxel, el estudio del escalado de la tensión de alimentación ha contribuido a mejorar la metodología de diseño para sensores de imagen CMOS de bajo voltaje, [14]. También cabe destacar la importancia de la aparición de nuevas configuraciones de píxel, como las denominadas estructuras de píxeles compartidos, en las que varios píxeles comparten la difusión flotante o algunos de sus transistores para reducir el área reservada a la electrónica y aumentar la capacidad del fotodiodo y la sensitividad [15, 16]. Igualmente interesantes son los estudios en los que se caracterizan y comparan diversos píxeles con diferentes combinaciones de fotodetector, transistores y arquitectura, para explorar las ventajas de cada uno de ellos [17, 18]. Así, por ejemplo, la tecnología de iluminación posterior (BSI) ha demostrado ser una buena solución para mejorar la relación señal-ruido [19].

A pesar de los progresos realizados a nivel de proceso y de píxel, la caracterización de sensores de imagen CMOS en tecnologías submicrométricas es escasa. Así, un estudio en los nodos tecnológicos de 0.18 μm y 0.15 μm con modificaciones menores presenta un sensor de imagen CMOS con excelente rendimiento que se caracteriza por su bajo ruido, alta sensitividad, alta velocidad, y funcionamiento en condiciones de baja iluminación, equiparable al estado del arte de los sensores de imagen CCD [20], contradiciendo los malos resultados en una tecnología CMOS estándar de 0.18 μm de hace ya más de una década [21]. De hecho, no sólo los píxeles caracterizados en una tecnología CIS de 0.18 μm han demostrado un buen comportamiento [22], sino también los de tecnologías estándar actuales de 0.18 μm [23, 24]. Más allá de procesos de 0.18 μm, se diseñaron estructuras de píxeles compartidos en procesos de cobre de 0.13 μm y 90 nm para estudiar su sensitividad [25]. También se desarrollaron sensores de imagen en tecnologías CMOS de 90 nm y 65 nm, evaluando nuevas configuraciones de píxel con fotodiodos apilados y alto factor de llenado que exhibieron características competitivas con sensores comerciales en tecnologías convencionales, [26].

A pesar de que es difícil satisfacer todas las características deseables en un diseño, tales como bajo nivel de ruido, alto rango dinámico, alta sensitividad, alto factor de llenado, bajo consumo de energía, operación a bajo voltaje e imagen de alta velocidad, el verdadero reto es mejorar el proceso tecnológico junto con el diseño de los píxeles para garantizar que no hay pérdida de rendimiento a medida que el tamaño del píxel se reduce, [27, 28]. Aunque los fabricantes de electrónica de consumo no suelen proporcionar información sobre el tamaño del píxel de sus productos, y por lo tanto es difícil saber cuál es el píxel más pequeño en el mercado, se estima que está muy por debajo de 2 μm, [29]. Sin embargo, todavía se echa en falta un estudio en profundidad de los principales fenómenos físicos que dominan el comportamiento de los píxeles en estos nodos tecnológicos. En particular, debe prestarse una mayor atención al impacto de la fotorrespuesta periférica en fotodiodos de pequeño tamaño, ya que existen estudios que predicen que su magnitud es comparable a la del área activa del píxel, [30]. Por esta razón, es necesario desarrollar modelos completos de la respuesta de los fotodiodos CMOS con el fin de permitir la elección correcta de la tecnología y la arquitectura de píxel. Por otra parte, desde el punto de vista industrial, el desarrollo de nuevos sensores CMOS no puede existir sin herramientas de diseño asistido por ordenador (CAD). Por lo tanto, son esenciales modelos compactos de fotodiodos CMOS incluyendo efectos periféricos en tecnologías submicrométricas que puedan ser incorporados a estas herramientas. En este sentido, el objetivo de este trabajo es proporcionar un estudio del comportamiento de fotodetectores de pequeño

tamaño en tecnologías CMOS avanzadas, a fin de evaluar el impacto del escalamiento en la fotorrespuesta del píxel.

La denominada captación periférica es la suma de la captación lateral y de fondo debidas a la difusión hacia la región de vaciamiento de las cargas fotogeneradas en el sustrato de los alrededores de la unión. Aunque los primeros estudios en relación a esta componente se remontan varias décadas atrás, el efecto de la captación periférica podía despreciarse cuando los fotodiodos eran de gran tamaño. El primer modelo semianalítico de la fotorrespuesta de un píxel CMOS incluyendo la captación periférica fue presentado en [31] y se utilizó para predecir la respuesta máxima del píxel al escalar la tecnología, [32]. Los mismos autores también estudiaron la respuesta periférica y la contaminación inter-píxel en una tecnología de 0.35 μm CMOS estándar mediante resultados experimentales y de simulación. Sin embargo, no se conocen estudios en nodos tecnológicos más actuales. Con este objetivo, en el trabajo que aquí se presenta se estudió la respuesta de la celda 3T-APS, ampliamente utilizada, por medio de medidas experimentales de diferentes píxeles con fotodiodos de unión p-n^+ y p-N_{well} en tecnologías de 180 nm CIS y 90 nm CMOS estándar, respectivamente. Así mismo, se derivó y validó un modelo semianalítico para su fotorrespuesta en términos de sensitividad. El modelo presta especial atención a la captación periférica, modelando este fenómeno como una componente diferente aparte de la captación del área activa. De este modo, se proponen y comparan varias funciones para modelar la contribución del área activa y del fondo de la unión. Los resultados se presentan en el Capítulo 2, que amplía el trabajo presentado en [33, 34, 35, 36].

El estudio preliminar sugiere que una mayor área activa no garantiza necesariamente la respuesta óptima para fotodiodos de pequeño tamaño. Por ello, posteriormente se llevó a cabo un estudio a nivel subpíxel para caracterizar las diferentes regiones por separado. Aunque existen estudios sobre el tamaño y la forma del píxel e incluso algunos modelos semianalíticos de la respuesta del píxel en función del área activa, pocos son los estudios subpíxel. De hecho, las medidas de este tipo requieren de un equipamiento óptico sofisticado y se necesita invertir un tiempo considerable para realizarlas correctamente. Uno de los primeros mapas de la fotorrespuesta a nivel subpíxel se presentó en [37]. Sin embargo, hoy en día la tecnología y el tamaño de los píxeles han quedado obsoletos. En [38] se encuentran medidas más recientes, aunque la tecnología tampoco es actual. La respuesta a una iluminación puntual también se estudió en detectores de infrarrojo, [39], y en fotodiodos BSI, [40]. El estudio a nivel subpíxel que se presenta en este trabajo consistió en la caracterización de la fotorrespuesta de

fotodiodos de unión p-n^+ y p-N_{well} fabricados en una tecnología de 90 nm CMOS estándar por medio de una fuente puntual de iluminación. Además, se propuso un modelo analítico para estimar la fotorrespuesta basado en la solución de la ecuación de estado estacionario en las diferentes regiones del dispositivo. El modelo propuesto muestra la importancia de la contribución lateral y fue comparado con éxito con los datos exprimentales. Otra prueba de la importancia de la captación lateral se encontró mediante la simulación de dispositivos bajo iluminación uniforme de los alrededores de la unión. Este análisis se detalla en el Capítulo 3 y fue presentado en [41].

Los estudios previos establecieron la importancia de la captación lateral en fotodiodos de pequeño tamaño, y de ahí la necesidad de encontrar una solución de compromiso entre el área activa y el área que rodea la unión para maximizar su respuesta. Es más, sería deseable disponer de un modelo que tenga en cuenta este fenómeno, y que pueda adaptarse fácilmente a diferentes tamaños y geometrías del fotodiodo y nodos tecnológicos. Sin embargo, no es sencillo contextualizar esta tarea dado que hay una gran variedad de modelos analíticos para fotodetectores en la literatura que pueden clasificarse en base a diferentes criterios tales como la dimensión (1D, 2D o 3D), el tipo de dispositivo (vertical, lateral, mesa, *finger*, iluminación trasera, etc.), el tipo de unión (p-n^+, n-p^+, p-N_{well}, N_{well}-p^+, p-epi-N_{well}, p-epi-P_{well}-n^+, etc.), el rango de aplicación (rayos gamma, rayos-X, ultravioleta, visible, infrarrojo, microondas, etc.), y otras características. Además, las condiciones de contorno y diversos tipos de simplificaciones pueden variar de un modelo a otro complicando aún más su clasificación.

Uno de los primeros modelos analíticos para fotodiodos basado en la resolución de la ecuación de continuidad en estado estacionario data de 1977, [42]. En él ya se hace mención a la captación periférica, aunque el tamaño de los dispositivos considerados es mucho mayor que el de los actuales. En cuanto a modelos bidimensionales de estructuras verticales, como las que son objeto de este trabajo, en [43] se hace una descripción cuantitativa de la fotocorriente de un fotodiodo p-n^+ basándose en [44] y particularizada para el caso de sustrato de película fino. Más allá de este análisis cuantitativo, en [45] se presentó un modelo para evaluar el impacto del tamaño del fotodiodo, el perfil de dopado y la velocidad de recombinación superficial en la eficiencia de una unión p-n^+, aunque no se deriva totalmente la expresión final, dificultando su aplicación práctica. Otro análisis bidimensional, pero limitado al sustrato, puede encontrarse en [46]. Finalmente, no se encuentran muchos trabajos que aborden esta problemática mediante la resolución de la ecuación de estado estacionario en tres dimensiones. En [47] se desarrolla un modelo analítico tridimensional para fotodiodos n-p^+ verticales

mediante un análisis de Fourier, bajo condiciones periódicas de iluminación y limitado al sustrato. Basándose en este trabajo, otro modelo en tres dimensiones para estructuras de fotodiodo periódicas se utilizó para ilustrar la importancia de la recombinación en superficie y la degradación de la movilidad a lo largo de la interfaz Si-SiO_2. En esta línea, y tras haber encontrado indicios sobre la importancia de la captación periférica en fotodiodos de pequeño tamaño, en este trabajo se presenta un modelo analítico para fotodiodos de unión p-n^+ verticales, operando en el rango visible y bajo iluminación uniforme, basado en la solución de la ecuación bidimensional de estado estacionario en los alrededores de la unión. El análisis se caracteriza por el tratamiento matemático que se ha hecho de la componente lateral. El modelo propuesto se ajusta con gran precisión a los resultados obtenidos mediante simulación y también fue validado posteriormente con medidas experimentales en tecnologías de 180 nm y 65 nm estándar. Este análisis se detalla en el Capítulo 4 y fue presentado en [48].

El modelo propuesto es compacto, general y escalable. En otras palabras, puede extenderse fácilmente a tamaños diferentes de fotodiodo, a otras geometrías y nodos tecnológicos. Con el fin de ser útil en herramientas para el diseño asistido por ordenador (CAD), el modelo fue implementado en un lenguaje de simulación hardware. De hecho, en la literatura no se han encontrado muchos trabajos acerca de la traducción a este tipo de lenguajes de modelos para fotodetectores y todos ellos son unidimensionales. Así, en [49] se presenta una colección de modelos para dispositivos optoelectrónicos, entre ellos un modelo de fotodiodo, aunque no se proporciona su expresión matemática y éste se basa en un dispositivo comercial. Por otro lado, en el marco del desarrollo de un simulador de circuitos de código abierto soportando el lenguaje Verilog-A, se sugiere un modelo de fotodiodo, pero no en función de parámetros físicos y tecnológicos y necesitando de un importante proceso de caracterización previo, [50]. Finalmente, en [51] se utilizan expresiones clásicas para el modelado de fotodetectores y píxeles en VHDL-AMS. Así, en el Capítulo 5 de este trabajo se muestra la implementación del modelo propuesto en un lenguaje de simulación hardware y su uso para la simulación de circuitos, ilustrando su potencialidad para la optimización del píxel. Un trabajo derivado de este estudio ha sido enviado para su publicación y se encuentra actualmente bajo revisión, [52]. También se aborda en este capítulo la implementación en Verilog-AMS de un modelo de transistor de puerta encerrada (ELT) desarrollado en trabajos previos [53, 54, 55].

Contribución

A continuación se resumen las principales conclusiones derivadas de este trabajo:

- Las medidas experimentales de celdas 3T-APS con fotodiodos de unión p-n^+ octogonales y p-N_{well} cuadrados en tecnologías de 180 nm CIS y 90 nm estándar de UMC, respectivamente, mostraron una dependencia de la sensitividad con la razón entre el área de captación activa y la periférica. Los fenómenos físicos en los alrededores de la unión se describen con un modelo semianalítico que se ajustó a los datos experimentales con gran precisión. Este hecho pone de manifiesto la correcta comprensión de la física del dispositivo y reveló la importancia de la captación lateral en fotodiodos de pequeño tamaño. Por lo tanto, la tendencia a maximizar el área activa del fotodetector con el propósito de obtener la máxima fotorrespuesta debe revisarse.

- Un estudio a nivel subpíxel permitió la caracterización de la fotorrespuesta de las distintas regiones del píxel. De esta forma, celdas 3T-APS con fotodiodos de unión p-n^+ y p-N_{well} cuadrados en una tecnología de 90 nm estándar de UMC fueron escaneados y medidos en términos de fotocorriente por medio de una fuente de iluminación puntual. Estas estructuras se modelaron mediante la solución analítica de la ecuación de estado estacionario en las diferentes regiones del píxel. Tanto el modelo como los datos experimentales muestran una importante fotorrespuesta debida a la iluminación del área de captación que rodea a la unión. Para confirmar este aspecto, se llevaron a cabo simulaciones de una unión p-n^+ para diferentes tamaños del área activa y manteniendo constante el tamaño total. Únicamente los alrededores de la unión fueron expuestos a la fuente de iluminación uniforme, mostrando una solución de compromiso entre las áreas de captación activa y periférica que optimizaba la respuesta. También se encontró que la respuesta del área periférica era más importante que la del área activa.

- Se propuso un modelo analítico para la fotorrespuesta lateral, basado en la resolución de la ecuación bidimensional de estado estacionario, que se ajustó de forma excelente a los resultados obtenidos mediante simulación. Posteriormente, las predicciones fueron validadas con medidas experimentales de fotodiodos de unión p-n^+ cuadrados en tecnologías estándar de 180 nm de AMS y de 65 nm de UMC. Para ello se caracterizaron fotodiodos con distinto tamaño del área activa y del área que rodea a la unión bajo iluminación uniforme. Para medir la fotorrespuesta periférica de forma indepen-

diente también se caracterizaron las mismas estructuras y en las mismas condiciones, pero con el área activa protegida frente a la luz. Los datos experimentales confirmaron el comportamiento pronosticado por las simulaciones, y el modelo propuesto reprodujo la respuesta de las estructuras en ambas tecnologías. Como resultado, se obtuvo un modelo para fotodiodos CMOS en el rango visible general, escalable y compacto.

– El modelo propuesto fue implementado en un lenguaje de descripción hardware y utilizado para la simulación de circuitos, demostrando ser una herramienta poderosa para el diseño asistido por ordenador de sensores de imagen CMOS. La potencialidad de este tipo de descripciones para el diseño de circuitos integrados que incluyen dispositivos no estándar fue también ilustrada mediante la implementación de modelos de transistores de topologías especiales de puerta encerrada.

Introduction

With camera manufacturers marketing their products with ever-increasing pixel counts, Complementary Metal-Oxide Semiconductor (CMOS) and Charge Coupled Devices (CCD) image sensors compete for existing and emerging market segments while at the same time trying to guarantee no loss of performance as the pixel size shrinks. The benefits of CMOS imagers were already predicted in the late 1990s [1], and they demonstrated a competitive behaviour over CCDs some years after [2]. Among the CMOS image sensors advantages, such as the system power and cost reductions, perhaps the miniaturization and the on-chip functionality are the most favoured by the CMOS technology scaling [3]. Advanced technological nodes represent the main course to achieve smaller pixels and thus high resolution in the same area. Even though the progress in CMOS technology offers the means to fabricate them, smaller pixels in advanced technologies must overcome some electrical and optical problems. In fact, although some studies were optimistic about the benefits of CMOS imagers around late 1990s, their quality beyond the 0.25 μm generation technology without any process change was questioned because scaling effects were expected to increase the leakage current and reduce the dynamic range [4]. Today, many of these problems have been minimized by advances in process engineering but the challenge to produce the smallest possible pixel with enough sensitivity remains. On the other hand, integrated photonic-electronic components are still dominated by the feature size reduction in CMOS technologies known as Moore's Law [5]. Because imagers must interact with light, Moore's Law impact differs from its impact on other integrated circuit applications. Thereby, how the trend towards smaller pixels interacts with the properties of light, such as photon noise and diffraction, must also be investigated.

Favoured by advances in technology fabrication, the market of CMOS image sensors has greatly increased over the last years. Parallel to this, a great concern has been raised in relation to the impact of technology and device scaling on the overall response [4], in particular in

terms of sensitivity [6], dark-current [7] and spectral response [8]. However, research on dimensional effects on ever-shrinking CMOS imagers is essential as efficient CMOS image sensor modelling and simulation represent a weak point of CMOS nano imager design. This deficiency needs to be addressed as it constitutes one of the few enabling methodologies that can reduce development cycle times and costs. Thus, an effort on a combined approach to process technology, pixel architecture and modelling for CMOS imagers to match CCD performance as pixel sizes shrink is needed [9].

In the last years, there have been significant efforts to modify the fabrication process of standard CMOS technologies to enhance their imaging performance, [10]. To improve photoresponsivity, nonsilicided deep junction diodes with optimized doping profiles have been included in standard processes. Dark current reduction is, on the other hand, achieved by means of nonsilicided, double-diffused source/drain implantation as well as pinned diode structures. Hydrogen annealing is also used to reduce leakage by passivating defects. The reduction of transistor leakage in both the reset and follower transistors in an active pixel sensor has been also considered through the use of thick gate oxides. Besides, the threshold voltage of the reset and follower transistors are increased and decreased to reduce its off-current and to improve voltage swing, respectively. Finally, after passivation, a color filter and microlenses can be formed on chip to improve quantum efficiency in CMOS Image Sensor (CIS) technologies.

Technology scaling also has detrimental effects on pixel optical efficiency that have been addressed by technology improvements [11]. For instance, light transmission is reduced by the use of silicon dioxide/nitride materials. Moreover, as CMOS technology scales, the distance from the surface of the chip to the photodetector increases relative to the size of the smallest pixel that can be fabricated. This is due to a slower reduction in the thickness of the interconnect layers, which scales less than the planar dimensions. As a result, light must travel through an increasingly deeper and narrower tunnel before reaching the photodetector surface. Thinning of metal and oxide layers is used to decrease the aspect ratio of the tunnel above each photodetector, [12]. On the other hand, oxide materials with better light transmission properties are being used to increase the optical efficiency. Another technique to increase the optical efficiency is the placement of air gaps around each pixel in order to create a rudimentary optical waveguide whereby incident light at the surface is guided to the correct pixel below via total internal reflection. The air gaps also serve to significantly reduce optical spatial crosstalk, which can be particularly problematic as pixel sizes decrease, [13]. All these process modifications have allowed the reduction of pixel size below predicted values.

Regarding the pixel architecture, research on the power supply voltage scaling has contributed to improve the design methodology for low voltage CMOS image sensors, [14]. Other studies have reported new pixel structures, the so-called shared pixels, in which several pixels share the floating diffusion or transistors to enhance photodiode capacity, sensitivity and fill factor [15, 16]. Photodetectors with different junctions in combination with different pixel transistors and architectures should also be explored to take advantage of their particular benefits, [17, 18]. In fact, Backside-Illuminated (BSI) technology has been recently adopted as a solution to improve pixel signal-to-noise ratio performance [19].

Despite the progress made at process and pixel level, there is a shortage of CMOS image sensors performance characterization in deep sub-micron technologies. For instance, contrary to the poor results of CMOS sensors in a 0.18 μm standard technology reported one decade ago in [21], a more recent study has demonstrated excellent CMOS imager low-noise, high-sensitivity, low-lag, and low-light performance, matching that of state-of-the-art CCD imagers in 0.18 μm and 0.15 μm technological nodes including minor process modifications [20]. In fact, not only tested pixels in 0.18 μm CIS technology have shown a good behaviour [22], but those in 0.18 μm standard technologies as well [23, 24]. Beyond 0.18 μm processes, shared pixels in 0.13 μm and 90 nm Cu processes were designed, respectively, to study their sensitivity in [25]. Image sensors using 90 nm and 65 nm CMOS technology were also developed, evaluating new pixel configurations with stacked photodiodes and high fill factor which exhibited characteristics competitive with commercial sensors in conventional technologies, [26].

All the desirable features, such as low noise, high dynamic range, high sensitivity, high fill factor, low power consumption, low voltage operation and high speed imaging, are difficult to achieve in one design, but the real challenge is to improve the technological process along with the pixel design to guarantee no loss of performance as the pixel size shrinks, [27, 28]. Although consumer electronics manufacturers do not usually provide pixel size information of their products and thus it is difficult to know what is the current smallest pixel in the market, its pitch has been reduced well under 2 μm thanks to the rapid scaling of CMOS technologies and the development of optimized image sensor processes for CMOS vision products [56]. However, an in-depth study of the main physical phenomena dominating the behaviour of pixels at these technological nodes is still missing. In particular, greater attention needs to be paid to the impact of the peripheral photoresponse on small photodiodes as its magnitude becomes comparable to that of the main active area of the pixel, [30]. For this reason, it is necessary to develop comprehensive models of the CMOS photodiodes response

in order to permit the proper choice of technology and pixel architecture. Furthermore, from an industrial point of view, the development of new CMOS sensor devices solutions cannot exist without computer-aided design (CAD) tools. Therefore, compact models of CMOS photodiodes including peripheral effects in sub-micron technologies are essential.

In this sense, the goal of this work is to provide a study of the behaviour of small photodetectors in advanced CMOS technologies in order to evaluate the impact of the geometry on the pixel photoresponse. With this aim, the response of the widespread used 3T-APS cell was studied by means of experimental measurements of different pixels with p-n^+ and p-N_{well} junction photodiodes in 180 nm CIS and 90 nm standard CMOS technologies, respectively. A semianalytical model for their photoresponse in terms of sensitivity was derived and validated. The model pays special attention to the peripheral collection, modelling this phenomenon as a different component apart from the active area collection. In this way, several functions to model the active area and bottom contributions are proposed and compared. The results are reported in Chapter 2 and summarized in [33, 34, 35, 36].

Since the preliminary study suggested that the largest active area no longer necessarily guarantees the optimum response for small photodiodes, a sub-pixel study was developed to study the different regions of the pixel separately. It consisted of the photoresponse characterization of p-n^+ and p-N_{well} junction photodiodes fabricated in a 90 nm standard CMOS technology by means of a point source illumination. An analytical model for the photoresponse estimation based on the solution of the steady-state equation in the different regions of the device was proposed and successfully compared with the experimental data, showing the significance of the lateral contribution. Further evidence of the importance of the lateral collection was found by device simulations under uniform illumination of the surroundings of the junction. This analysis is detailed in Chapter 3 and was presented in [41].

The previous studies established the importance of the lateral collection in small photodiodes and hence the need to find a trade-off between the active area and the collecting area surrounding the junction to maximize the response. Based on the solution of the two-dimensional steady-state equation in the surroundings of the junction, an analytical model for uniformly illuminated p-n^+ junction photodiodes was proposed. The model fitted device simulation results with excellent agreement and was also validated with experimental measurements in 180 nm and 65 nm standard technologies. This part of the work is covered by Chapter 4 and was presented in [48].

The proposed model is compact, general and scalable. In other words, it can be easily extended to different photodiode sizes, geometries and technological nodes. In order to be used in Computer Aided Design (CAD) tools, the model was implemented in a Hardware Description Language (HDL) and used for circuit simulations to illustrate the potential of the model for the optimization of the pixel performance. More details are given in Chapter 5 and have been summarized in [52].

CHAPTER 1

SOLID-STATE IMAGE SENSORS

A solid-state image sensor, also called an imager, is a semiconductor device that converts an optical image into electronic signals. A high quality image is achieved through high resolution, high sensitivity, high speed imaging, wide dynamic range, good linearity for colour processing, low power consumption, low voltage operation and very low noise.

The number of applications using image sensors is growing rapidly. They can detect light within a wide spectral range, from X-rays to infrared wavelength regions, by tuning its detector structures and employing materials which are sensitive to the wavelength region of interest. However, the focus of this work is on visible imaging, corresponding to the spectral response of the human eye, which responds to wavelengths from about 390 to 750 nm. Silicon, the most widely used material for Very Large-Scale Integrated circuits (VLSIs), is also suitable for image sensors on the visible range because the band gap energy of silicon matches the energy of visible wavelength photons.

This chapter reviews the basics of image sensors, their evolution and the current technologies used for their fabrication. Based on this, the framework of this work is presented.

1.1 Evolution

The earliest solid-state image sensors were the bipolar and MOS photodiode arrays developed by Morrison [57], IBM [58] and Westinghouse [59] in the 1960s. All these sensors had an output signal proportional to the instantaneous local incident light intensity and did not perform any intentional integration of the optical signal. As a consequence, the sensitivity of these devices was low and they required gain within the pixel to enhance their performance.

In 1967, Weckler at Fairchild suggested operating p-n junctions in a photon flux integrating mode [60], where the photocurrent from the junction was integrated on a reverse-biased p-n junction capacitance and readout of the integrated charge using a PMOS switch was suggested. The signal charge, appearing as a current pulse, could be converted to a voltage pulse using a series resistor. A 100×100 element array of photodiodes was reported in [61]. Also in 1967, RCA Laboratories reported a Thin-Film Transistor (TFT) solid-state image sensor using TFTs and photoconductors [62]. The 180×180 element array included self-scanning complementary logic circuitry for sequentially addressing pixels. Several configurations of self-scanned silicon image detector arrays were reported by Noble at Plessey in 1968 [63]. Noble also discussed a charge integration amplifier for readout, similar to that used later by others. In addition, the first use of a MOS source-follower transistor in the pixel for readout buffering was proposed. An improved model and description of the operation of the sensor was reported by Chamberlain in 1969 [64].

The issue of Fixed-Pattern Noise (FPN) was explored in 1970 by Fry, Noble, and Rycroft and it was considered the primary problem with MOS and CMOS image sensors until late 1990s, [65]. Invented in 1970 as an analog memory device [66], CCD quickly became the dominant image sensor technology. Its relative freedom from FPN was one of the major reasons for its adoption over the many other forms of solid-state image sensors. The smaller pixel size afforded by the simplicity of the CCD pixel also contributed to its adoption by industry. Thus, CMOS image sensors could not compete with CCD technology in the past because of poor performance and large pixel size for that time relative to that of the CCDs.

Thereby, while a large effort was applied to the development of the CCDs in the 1970s and 1980s, MOS image sensors were only sporadically investigated and compared unfavourably to CCDs. In the late 1970s and early 1980s Hitachi and Matsushita continued the development of MOS image sensors for video camera recorder applications [67, 68]. Temporal noise in MOS sensors started to fall behind the noise achieved in CCDs, and by 1985, Hitachi combined the MOS sensor with a CCD horizontal shift register [69]. In 1987, Hitachi introduced a simple on-chip technique to achieve variable exposure times and flicker suppression from indoor lighting [70]. Despite these advances and perhaps due to residual temporal noise, Hitachi gave up its MOS approach to sensors.

In the late 1980s, while CCDs predominated in visible imaging, two related fields started to turn away from the use of CCDs. The first was hybrid infrared focal-plane arrays that initially used CCDs as a readout multiplexer. Due to limitations of CCDs, particularly in

low-temperature operation and charge handling, CMOS readout multiplexers were developed which allowed both increased functionality as well as performance compared to CCD multiplexers. A second field was high-energy physics particle/photon vertex detectors. Many designers in this area also initially used CCDs for detection and readout of charge generated by particles and photons. However, the radiation sensitivity of CCDs and the increased functionality offered by CMOS has led to subsequent abandonment of CCD technology for this application. Despite this, full-analog CCDs continued to dominate vision applications owing to their superior dynamic range, lower FPN, smaller pixel size and higher sensitivity to light [71].

In the early 1990s, two independently motivated efforts led to a resurgence and significant advances in CMOS image sensor development. The first effort was to create highly functional single-chip imaging systems where low cost was the driving factor. This effort was headed by separate researchers at the Universities of Edinburgh and Linkoping. The second independent effort grew from NASA's need for highly miniaturized, low-power, instrument imaging systems for next-generation deep-space exploration spacecraft. Such imaging systems are driven by performance, not cost. Until then the Passive Pixel Sensor (PPS) had been the CMOS image sensor technology of choice [72]. The feature sizes of the available CMOS technologies were too large to accommodate more than a single transistor and some interconnect lines in a PPS. However, PPSs had much lower performance than CCDs, which limited their applicability to low-end machine-vision applications. In the early 1990s, work began on the modern CMOS Active Pixel Sensor (APS), conceived originally in 1968 [63]. It was quickly realized that adding an amplifier to each pixel significantly increases sensor speed and improves its Signal-to-Noise Ratio (SNR), thus overcoming the deficiencies of PPS.

CMOS technology feature sizes, however, were still too large to make APS commercially viable. With the coming of deep sub-micron CMOS and integrated microlens technologies, APS made CMOS image sensors a viable alternative to CCDs. Taking further advantage of technology scaling, the Digital Pixel Sensor (DPS), first reported in [73], integrates an ADC at each pixel. The massively parallel conversion and digital readout provide very high speed readout, enabling new applications such as wider dynamic range imaging.

Around 2000 the research was mainly focusing on the improvement of the APS because it had shown better performance and flexibility. In order to strongly compete with CCD technology, the aim of researchers was to obtain higher performance imaging systems based on CMOS technology. Therefore, there were several reports on improving the Fill Factor

(FF) with low power consumption, low voltage operation, low noise, high speed imaging and high dynamic range. Besides, little research was done on other topics such as pixel shape optimization [31], pixels on Silicon On Insulator (SOI) substrate [74], APS with variable resolution [75], self-correcting [76] and low light conditions [77]. On the other hand, new applications emerged due to the CMOS imager development. Automotive applications, imaging for cellular or static phones, computer video, space, medical, digital photography and 3D applications were improved. So many application areas caused that CMOS technology made a breakthrough on two fronts in 2000: sensors for computers and cell phones on the low end, and ultra high speed, large format imaging on the high-end. Furthermore, new technologies and architectures appeared due to scale effects, as the Thin Film on ASIC (TFA) technology and Complementary Active Pixel Sensors (CAPS). Finally, some studies have been carried out to study the cross-contamination between CIS (CMOS Image Sensor) and IC technologies [78] and the radiation and hot carriers effects [79, 80].

In recent years, the reduction of pixel size in CMOS image sensors has become even more important than in CCD image sensors. The first of the strategies for reducing pixel size is reducing the number of transistors in the pixel, which has been made possible by sharing transistors between pixels, [81]. The second is to effectively guide the incident light to the photodiode, and towards this end, firstly, microlenses are placed over the sensor and, secondly, the thickness of the interconnect section is reduced by switching from aluminium to copper as the interconnect material. The column-parallel A/D conversion technique, which includes dual noise reduction circuits that suppress the noise generated in each pixel, was developed for high-speed readout. This technique allows CMOS image sensors to achieve frame rates 20 times or more faster than those in CCD image sensors. Finally, progress in sensitivity has been made possible by the back-illuminated structure, which offers higher sensitivity and lower noise.

The current goal for CMOS image sensor development is exceeding human vision. Compared to CCD image sensors, CMOS image sensors allow the implementation of system functions on the same chip. This is why CMOS image sensors are used in almost all cellular phone cameras. Also, the reason they are used in high-resolution video camera recorders is that they support low-power operation and high-speed image readout. The main points in CMOS image sensor development are how to make their advantages even better and how to reduce their noise and sensitivity disadvantages.

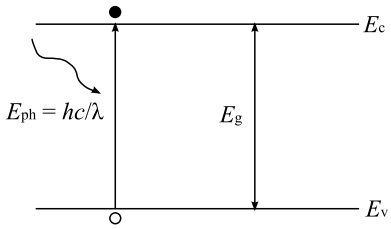


Figure 1.1: Photogeneration

1.2 Basics

1.2.1 Photoconversion

The optical absorption is a process used to convert optical energy into electronic energy. Electron-hole pairs generation takes place when a flux of photons enters a semiconductor at energy levels that exceed the semiconductor band gap energy, E_g, such that

$$E_{ph} = h\nu = \frac{hc}{\lambda} \geq E_g \tag{1.1}$$

where h, ν, c, and λ are Planck's constant, the frequency of light, the speed of light, and the wavelength of light, respectively (Figure 1.1). Because the band gap energy of silicon is 1.124 eV, light with wavelengths shorter than 1100 nm is absorbed and photon-to-signal charge conversion takes place. On the other hand, silicon is essentially transparent to photons with wavelengths longer than 1100 nm.

The number of photogenerated electron-hole pairs per unit volume and time is the optical generation rate, $G(y)$,

$$G(y) = -\frac{\partial \Phi}{\partial y} \tag{1.2}$$

where Φ is the photon flux and y is the depth in silicon. According to the Beer's law, Φ decays exponentially with y as follows

$$\Phi(y) = \Phi_0 e^{-\alpha y} \tag{1.3}$$

where Φ_0 is the photon flux at the silicon surface and α is the absorption coefficient.

The photon flux at the surface can be written as

$$\Phi_0 = \frac{P_{opt} T_c \lambda}{hc} \tag{1.4}$$

Parameter	Value	Units
ε_1	1.09969	eV
$d\varepsilon_1$	0.0583148	eV
C_{1+1}	483.916	eV/cm
C_{1-1}	5030.02	eV/cm
$d\varepsilon_2$	0.0220161	eV
C_{2+1}	79.4079	eV/cm
C_{2-1}	1634.30	eV/cm
ε_3	1.40985	eV
C_3	1.40985	eV
dN	1.23084	eV^{-1}
N	0.394122	-

Table 1.1: Equation (1.5) parameters to describe the absorption coefficient of silicon

where P_{opt} represents the incident optical power and T_{c} the transmission coefficient, which is calculated using the Fresnel equations under normal incidence, see Section 1.2.10.

The absorption coefficient of silicon at room temperature is modelled as a function of the impinging radiation wavelength given by [82],

$$\alpha(\lambda) = \frac{1}{E_{\text{ph}}}\left[\sum_{i=1}^{2}\sum_{j=-1}^{1}\left(\frac{C_{ij}}{4}\left(E_{\text{ph}} - \varepsilon_1 + jd\varepsilon_i + |E_{\text{ph}} - \varepsilon_1 + jd\varepsilon_i|\right)^2\right) + \right. \\ \left. + C_3\left(E_{\text{ph}} - \varepsilon_3 + |E_{\text{ph}} - \varepsilon_3|\right)^{N+dNE_{\text{ph}}}\right] \tag{1.5}$$

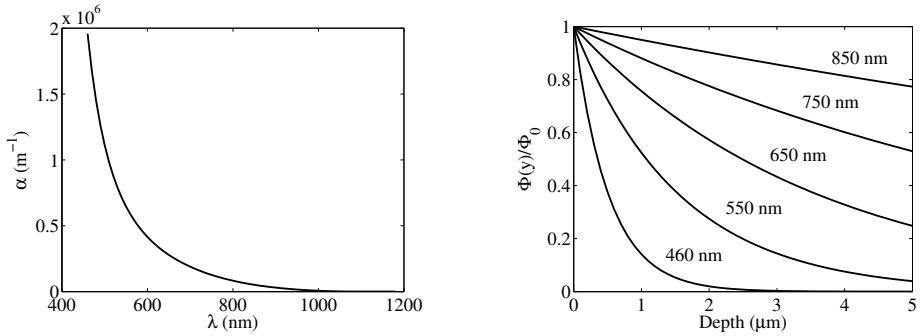
where $j \neq 0$ and 460 nm $< \lambda <$ 1185 nm. The values of the other parameters are given in Table 1.1. It can be observed in Figure 1.2(a) that the absorption coefficient decreases for longer wavelengths, which means less photon flux decay at the same depth, Figure 1.2(b).

1.2.2 Charge collection efficiency

Charge collection efficiency, $\eta(\lambda)$, characterizes the photoconversion at the detector and is defined by

$$\eta(\lambda) = \frac{\text{Signal charge}}{\text{Photogenerated charge}} \tag{1.6}$$

A sensor based on the optical absorption principle is needed to separate efficiently the electron-hole pairs and collect them. This is done by an electric field which can be either internal or externally applied. The photogenerated charge inside the depletion region is fully



(a) Absorption coefficient.

(b) Decay of the photon flux.

Figure 1.2: Absorption of light in silicon at room temperature.

utilized as signal charge. However, only a fraction of the photogenerated charge in the neutral region deep in the bulk can reach the depletion region through diffusion because no electric field exists at the neutral region and some of the electrons are lost by the recombination process before reaching the depletion region. Recombination is another mechanism which occurs in parallel with the optical generation and is proportional to the number of holes and electrons. The movement of the signal charge due to the electric field produces the measured photocurrent.

Summarizing, charge collection efficiency depends on the substrate type, impurity profile, minority carrier lifetime in the bulk, and how the photodetector is biased.

1.2.3 Quantum Efficiency (QE), Responsivity (R) and Sensitivity (S)

Spectral response is often described in terms of its external Quantum Efficiency (QE), which is defined as the ratio of absorbed photocarriers, $N_{\text{sig}}(\lambda)$, to the number of injected photons, $N_{\text{ph}}(\lambda)$, for a specific wavelength [83],

$$\text{QE}(\lambda) = \frac{N_{\text{sig}}(\lambda)}{N_{\text{ph}}(\lambda)} \tag{1.7}$$

where

$$N_{\text{sig}} = \frac{J_{\text{ph}} A_{\text{pix}} t_{\text{int}}}{q} \tag{1.8}$$

$$N_{\text{ph}} = \frac{P_{\text{opt}} A_{\text{pix}} t_{\text{int}}}{h\nu} \tag{1.9}$$

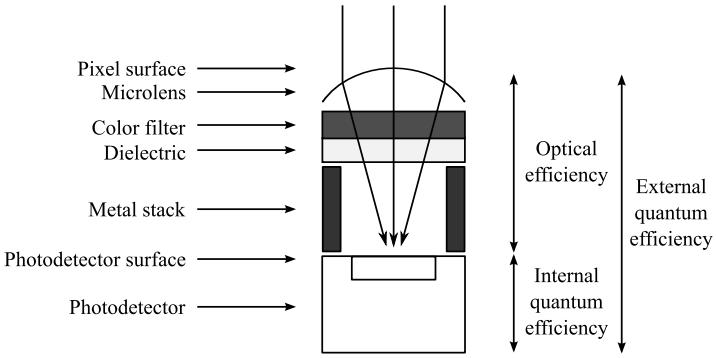


Figure 1.3: Cross-section scheme of a pixel.

and q, J_{ph}, A_{pix} and t_{int} are the electron charge, the photocurrent density, the pixel area and the integration time, respectively.

External QE can be expressed as the product of optical efficiency and internal QE, Figure 1.3. Optical efficiency describes the pixel capacity to absorb or reflect photons because of the upper structures above the photodetector. The shape and size of the aperture, the length of the dielectric tunnel through which light must travel before reaching the photodetector, and position, shape, and size of the photodetector, all determine the optical efficiency. Thus, optical efficiency is the photon-to-photon efficiency from the pixel surface to the photodetector surface. On the other hand, internal QE is the fraction of photons reaching the photodetector surface which contributes to the photocurrent. It is a function mainly of photodetector geometry and doping concentrations. In conclusion, Equation (1.7) can be also expressed as

$$\text{QE}(\lambda) = T_{\text{c}}(\lambda)\,\text{FF}\,\eta(\lambda) \tag{1.10}$$

where the transmission coefficient (T_{c}) and the effective Fill Factor (FF) are defined in Section 1.2.10 and Section 1.2.9, respectively.

External quantum efficiency can be also written in terms of the responsivity, $R(\lambda)$, as

$$\text{QE}(\lambda) = R(\lambda)\frac{hc}{q\lambda} \tag{1.11}$$

where $R(\lambda)$ is defined as the ratio of the photocurrent to the optical input power and is given by

$$R(\lambda) = \frac{J_{\text{ph}}}{P_{\text{opt}}} = \frac{qN_{\text{sig}}(\lambda)}{h\nu N_{\text{ph}}(\lambda)} \tag{1.12}$$

Finally, another important performance indicator in image sensors is the photometric sensitivity, $S(\lambda)$, which determines the output signal of the image sensor illuminated by a certain light level within a specific integration time. This magnitude is expressed in volts per lux-second, electrons per lux-second, bits per lux-second, etc. S can be expressed as the product of two terms: the conversion gain, CG (Section 1.2.4), and the responsivity,

$$S(\lambda) = CG \times R(\lambda) \tag{1.13}$$

1.2.4 Full-well capacity, capacitance (C_{PD}) and Conversion Gain (CG)

A photodetector operating in the charge-integrating mode has a limited charge handling capacity. The maximum amount of charge that can be accumulated on a photodetector capacitance is called full-well capacity or saturation charge and is given by

$$N_{\mathrm{sat}} = \frac{1}{q}\int_{V_{\mathrm{reset}}}^{V_{\mathrm{max}}} C_{\mathrm{PD}}(V)\mathrm{d}V \tag{1.14}$$

where C_{PD} is the photodetector capacitance and the reset and maximum voltages, V_{reset} and V_{max}, depend on photodetector structure and the operating conditions.

The capacitance is defined as

$$C = \frac{\mathrm{d}Q}{\mathrm{d}V} \tag{1.15}$$

where Q and V are the charge and the bias voltage of the device. A p-n junction exhibits two types of capacitance, the diffusion and the depletion capacitances.

The diffusion capacitance is due to minority carriers and it is sometimes called charge storage capacitance. It is related to charge that is stored in the diode when it is forward biased. Forward bias of the diode causes the diode to conduct current, which implies that a certain amount of charge is transported through the diode per unit time. If the diode voltage varies, the charge will change to the value required at the new operation point. This change in stored charge with diode voltage is the diffusion capacitance.

The depletion capacitance, on the other hand, is due to charges of dopants and it is sometimes called junction capacitance. It is determined by the spacing between the positive charge on the p-side of the junction and the negative charge on the n-side, that is, the depletion region, which depends on the junction voltage. The majority carriers are added or removed from the borders of the depletion region when the junction reverse voltage variation is positive or negative, respectively. Thus, the depletion region width decreases or increases in accordance with

this. Since the incremental charge diagrams are similar to the carrier fluctuations of a parallel-plate capacitor, the depletion capacitance is calculated as the capacitance of a parallel-plate capacitor with a distance between the plates equal to the depletion region width.

Generally, the diffusion capacitance in forward-bias operation is much larger than the depletion capacitance and the latter can be neglected for forward-biased junctions. However, the diffusion capacitance due to the minority carriers only affects in forward-bias operation and, consequently, can be neglected in reverse-bias operation, the photodetector common mode of operation. Thus, the photodetector capacitance is defined as the depletion capacitance due to the majority carriers, which is the sum of the junction bottom area and junction side-wall capacitances,

$$C_{\mathrm{PD}} = \frac{K_{\mathrm{s}}\varepsilon_0}{W}A + \frac{K_{\mathrm{s}}\varepsilon_0}{W_\ell}A_{\mathrm{P}} \tag{1.16}$$

where,

K_{s}	silicon dielectric constant;
ε_0	vacuum permittivity;
W, W_ℓ	vertical and lateral depletion region width, respectively;
A, A_{P}	photodetector junction bottom area and junction side-walls, respectively.

The depletion region width and thus the capacitance value are mainly determined by the doping profile. Using abrupt junction approximation, Equation (1.16) can be rewritten as,

$$C_{\mathrm{PD}} = \frac{K_{\mathrm{s}}\varepsilon_0}{\sqrt{\frac{2K_{\mathrm{s}}\varepsilon_0}{q}\left(\phi_{\mathrm{B}} - V_{\mathrm{PD}}\right)\left(\frac{N_{\mathrm{A}}+N_{\mathrm{D}}}{N_{\mathrm{A}}N_{\mathrm{D}}}\right)}}A + \frac{K_{\mathrm{s}}\varepsilon_0}{\sqrt{\frac{2K_{\mathrm{s}}\varepsilon_0}{q}\left(\phi_{\mathrm{BP}} - V_{\mathrm{PD}}\right)\left(\frac{N_{\mathrm{A}}+N_{\mathrm{D}}}{N_{\mathrm{A}}N_{\mathrm{D}}}\right)}}A_{\mathrm{P}} \tag{1.17}$$

where,

ϕ_{B}, ϕ_{BP}	built-in potential of the bottom area and side-walls, respectively;
V_{PD}	photodetector bias voltage;
N_{A}, N_{D}	acceptor and donor doping concentration, respectively.

Finally, it is very common to write the depletion capacitance as,

$$C_{\mathrm{PD}} = C_{\mathrm{A}}A + C_{\mathrm{P}}A_{\mathrm{P}} \tag{1.18}$$

where,

$$C_A = \frac{C_{\mathrm{JO}}}{\left(1 - \frac{V_{\mathrm{PD}}}{\phi_{\mathrm{B}}}\right)^{M_{\mathrm{J}}}} \tag{1.19}$$

$$C_{\mathrm{P}} = \frac{C_{\mathrm{JOP}}}{\left(1 - \frac{V_{\mathrm{PD}}}{\phi_{\mathrm{BP}}}\right)^{M_{\mathrm{JP}}}} \tag{1.20}$$

and,

C_{A}, C_{P}	unit junction bottom area and junction side-wall capacitances;
C_{JO}, C_{JOP}	unit zero-bias junction bottom area and junction side-wall capacitances;
M_{J}, M_{JP}	junction grading coefficients of the bottom area and side-walls.

The capacitance at the sensing node determines the charge capacity and the charge-to-voltage conversion gain of the image sensors, CG. The conversion gain is a measure of the increase of the photodetector voltage according to the amount of accumulated charge and is inversely proportional to the total capacity of the photodetector,

$$CG = \frac{q}{C_{\mathrm{PD}}} \tag{1.21}$$

A smaller capacitance at the charge sensing node is usually favoured since it provides a higher signal-to-noise ratio of the output signal. However, the drawback is a lower dynamic range.

1.2.5 Signal-to-Noise Ratio (SNR), Dynamic Range (DR) and crosstalk (CTK)

Signal-to-Noise Ratio (SNR) is the ratio of the signal to the noise, N_{noise}, at a given input level. It measures the quality of the signals produced by the sensor within the detection range,

$$\mathrm{SNR} = 20\log\left(\frac{N_{\mathrm{sig}}}{N_{\mathrm{noise}}}\right) \tag{1.22}$$

Dynamic Range (DR) quantifies the range of illumination that can be detected by the image sensor. Thus, DR is defined as the ratio of the saturation signal (full-well capacity), N_{sat}, to the minimum detectable signal, N_{min},

$$\mathrm{DR} = 20\log\left(\frac{N_{\mathrm{sat}}}{N_{\mathrm{min}}}\right) \tag{1.23}$$

Crosstalk (CTK) is the phenomenon by which photocarriers are collected by a photodetector due to the illumination of a neighbour. There are two physical mechanisms that may cause crosstalk. Optical crosstalk results from the multiple reflection, refraction and scattering of

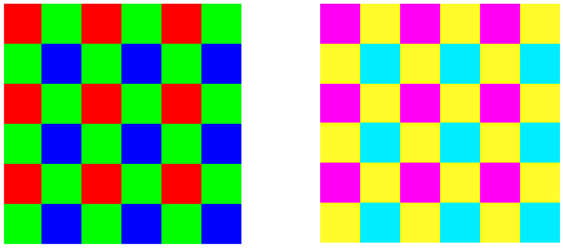


Figure 1.4: Bayer and CMY complementary colour pattern filters.

radiation between different surfaces within the chip. Electrical crosstalk within the photodetectors, on the other hand, is the phenomenon whereby the photocarriers generated deep in the photoconversion area by long wavelength light may diffuse into neighbouring pixels. The crosstalk degrades the spatial resolution, reduces the sensitivity, makes poor color separation, and leads to additional noise in the image after color correction procedure.

1.2.6 Modulation Transfer Function (MTF)

Measuring the Modulation Transfer Function (MTF) is a technique used to characterize a system frequency response or resolving capability. The MTF of an image sensor is the magnitude of the Fourier transform of the sensitivity distribution inside a pixel. Higher MTF is obtained from a narrower sensitivity distribution.

In a image system, the lens system, the optical components, the image sensor, and the image-processing block are cascaded to form the total MTF. The total system MTF is simply the product of the individual MTFs of each component.

1.2.7 Colour Filter Array (CFA)

An image sensor is basically a monochrome sensor responding to light energies that are within its sensitive wavelength range. Thus, a method for separating colours must be implemented in an image sensor to reproduce an image of a colour scene. As it is shown in the cross-section scheme of a pixel in Figure 1.3, an on-chip Colour Filter Array (CFA) built above the photodiode array provides a cost-effective solution for separating colour information and meeting the small size requirements.

The generation of a colour image requires three primary colours (red, green and blue or cyan, magenta and yellow) for each pixel. The CFA filters the light by wavelength, making the colour distinction possible. The original data of each pixel only contain the information of one of the colours, depending on the filter located over it. A colour pixel is the result of the interpolation of the pixels associated with the three colours and the quality of the final image is highly dependent on the chosen algorithm.

Many applications use the red, green, and blue (RGB) primary colour filter array. The most commonly used primary colour filter pattern is the Bayer pattern, shown in the left part of Figure 1.4. Proposed by B.E. Bayer [84], this pattern configuration has twice as green filters as blue or red filters. This is because the human visual system derives image details primarily from the green portion of the spectrum. That is, luminance differences are associated with green whereas colour perception is associated with red and blue.

Figure 1.4 shows also the CMY complementary colour filter pattern consisting of cyan, magenta, and yellow colour filters. The transmittance range of each complementary colour filter is broad, and higher sensitivity can be obtained compared to RGB primary colour filters. However, colour reproduction quality is usually not as accurate as that found in RGB primary filters.

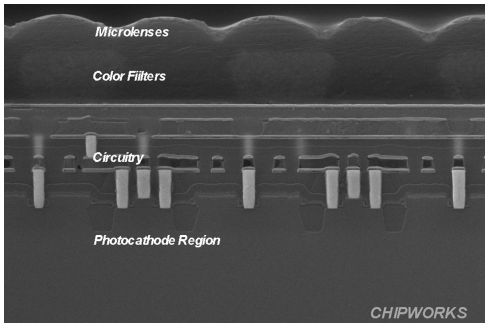
1.2.8 On-chip Microlens Array (OMA)

Microlenses are tiny lenses placed over the sensor and the colour filter, Figure 1.3. On-chip Microlens Array (OMA) collimates incident light to the ever shrinking photodetector area to improve the sensitivity of the pixel and the quality of those which present a low fill factor (Section 1.2.9). Thus, the microlens layer is another important factor for the technology scaling of the pixel.

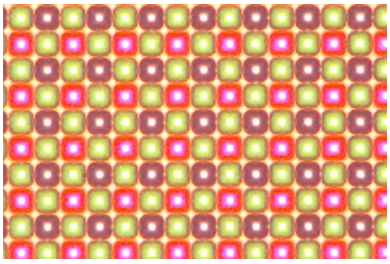
As Figure 1.3 depicts, if the thickness of the layers located over the photodetector is not scaled, the microlens focal distance must be the same independently of the pixel size. This fact requires the flexibility of adapting the microlens radius independently of their size. However, the scaling of the pixel size has an optical limit which is defined by the diffraction and aberration both in the lens system of the camera and the microlens. The lens resolution is limited by diffraction as:

$$r = 1.22\lambda F \tag{1.24}$$

where r is the radius of the first dark ring and F is the F-number. As the diffraction increases with F and low values of F produce high incident angles making more interference, the useful



(a) Internal structure of an OmniVision sensor reproduced from Chipworks.



(b) On-chip Microlens Array (OMA) and Colour Filter Array (CFA).

Figure 1.5: Microlenses.

range of F is very limited. However, camera lenses are usually limited by aberration for low values of F, which means a practical pixel size around 2.2-2.5 μm. On the other hand, aberrations can be reduced by advanced lens process while the effect of diffraction due to the limit of lens size cannot be avoided.

A photograph of the internal structure of a microlens is shown in Figure 1.5(a) and Figure 1.5(b) represents the combined effect of the microlenses and the colour filter array.

1.2.9 Fill Factor (FF)

Fill Factor (FF) is defined as the ratio of the photosensitive area inside a pixel, A, to the pixel area, A_{pix}. That is,

$$\text{FF} = \frac{A}{A_{\text{pix}}} \tag{1.25}$$

Without an on-chip microlens, it is defined by the aperture area not covered with a light shield. Thereby, if more transistors are used, the FF is degraded accordingly. The microlens condenses light onto the photodetector and effectively increases the FF. The microlens plays a very important role in improving light sensitivity on CCDs and CMOS image sensors. However, the CCD FF is usually higher than that of CMOS image sensors because the latter include transistors within the pixel, as explained in Section 1.3.

1.2.10 Reflection (R_c) and Transmission (T_c) coefficients

Incident light is reflected at the interface of two materials when their refractive indexes are different. Reflection (R_c) and transmission (T_c) coefficients of light rays that incide perpendicularly on the materials are given by the Fresnel equations [85]:

$$R_c = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{1.26}$$

and

$$T_c = \frac{4n_1 n_2}{(n_1 + n_2)^2} \tag{1.27}$$

where n_1 and n_2 are the refractive indexes of the two materials.

1.2.11 Noise

Noise deteriorates the imager performance and determines the sensitivity of an image sensor. Therefore, the term noise in image sensors may be defined as any signal variation that deteriorates an image or signal. There are several noise sources in an optical detection system. Noise is present in the signal and the background. There are imager internal noise sources which can be amplified. There is also noise in the amplification stages and the circuitry/electronics in general.

The sources of noise in photodetectors can be classified into two categories: spatial or fixed-pattern noise and temporal noise, [83]. The fixed-pattern noise describes the spatial variation of the image plane when an uniform illumination is applied, while the temporal noise is random and describes the temporal variations of the output signal. The former is purely deterministic and the latter is probabilistic.

Spatial Noise or Fixed-Pattern Noise (FPN)

Noise appearing in a reproduced image, which is fixed at certain spatial positions, is referred to as Fixed-Pattern Noise (FPN). FPN is also seen under uniform illumination conditions.

The primary FPN component in a CCD image sensor is dark current nonuniformity. In CMOS image sensors, the main sources of FPN are dark current nonuniformity and performance variations of an active transistor inside a pixel. Dark current is an undesirable current which is observed when the subject image is not illuminated. It is proportional to the integration time and is also a function of temperature. The three primary dark current components

are the generation in the depletion region, the diffusion from a neutral bulk and the generation at the surface of the photodetector. Although it is barely noticeable in normal modes of operation, it can be seen in images that have long exposure times or which were taken at high temperatures. If the dark current of each pixel is not uniform over the whole pixel array, the nonuniformity is seen as FPN. The dark charge reduces the imager dynamic range because the full well capacity is limited. It also changes the output level that corresponds to no illumination conditions. However, FPN at dark can be removed, in principle, by signal processing because it is fixed in space.

Shading is a slowly varying or low spatial frequency output variation seen in a image. The main sources of shading include dark-current-oriented, microlens-oriented and electrical-oriented shading. In CMOS image sensors, nonuniform biasing and grounding may cause shading.

Temporal Noise

Temporal Noise (TN) is a random variation in the signal that fluctuates over time. TN is frozen as spatial noise when a snapshot is taken. However, although temporal noise is fixed spatially in a particular shot, it will vary in sequential shots.

Three types of fundamental TN mechanisms exist in optical and electronic systems: thermal noise, shot noise, and flicker noise. In image sensors there are also other temporal noise sources such as the reset noise or KTC and read noise.

Thermal noise comes from thermal agitation of electrons within a resistance. It is also referred to as Johnson noise because it was discovered by J.B. Johnson in 1928. Nyquist described the noise voltage mathematically using thermodynamic reasoning the same year.

Shot noise is generated when a current flows across a potential barrier. In image sensors, shot noise is associated with incident photons and dark current. A study of the statistical properties of shot noise shows that the probability that particles are emitted during a certain time interval is given by the Poisson probability distribution. The power spectral densities of thermal noise and shot noise are constant over all frequencies, therefore being often referred to as white noise.

Flicker noise is also called 1/f noise because its power spectral density is proportional to 1/f, where f is the signal frequency. The average over time of 1/f noise may not be constant. It is associated with a phenomenon of charges trap and emission to and from the impurity states in the surfaces and interfaces of the contacts. This noise source is process dependent

and it is reduced by process optimization. The output amplifier of CCD image sensors and the amplifier in a CMOS image sensor pixel suffer from 1/f noise at low frequencies. However, 1/f noise is mostly suppressed by Correlated Double Sampling (CDS) as long as the CDS operation is performed in such a way that the interval between the two samples is short enough so that the 1/f noise is considered an offset.

When a floating diffusion capacitance is reset, reset or KTC noise appears at the capacitance node when the MOS switch is turned OFF. This noise comes from the thermal noise of the MOS switch.The KTC noise that appears in the floating diffusion amplifier in CCD image sensors can be suppressed by a CDS circuit. In CMOS image sensors, the KTC noise appears at the reset of the charge-detecting node. Suppressing KTC noise through CDS in CMOS sensors depends on the pixel configuration.

Read noise, or noise floor, is defined as noise that comes from the readout electronics. Noise generated in a detector is not included. In CCD image sensors, the noise floor is determined by the noise generated by the output amplifier, assuming that the charge transfer in the CCD shift registers is complete. In CMOS image sensors, the noise floor is determined by the noise generated by readout electronics, including the amplifier inside the pixel.

Smear and Blooming

These phenomena occur when a very strong light illuminates an imager. Smear is a typical phenomenon of CCD image sensors and it appears as a white vertical stripe image. Blooming occurs when the photogenerated charge exceeds a pixel full-well capacity and spills over to neighbouring pixels. CCD image sensors are also more affected by this phenomenon.

Image lag

Image lag is a phenomenon in which a residual image remains in the following frames after the light intensity suddenly changes. Lag can occur if the charge transfer from the photodiode in a CCD is not complete. In a CMOS 4T-APS, this can be caused by an incomplete charge transfer from the photodiode to the floating diffusion, while it appears when the pixel operates in soft reset mode in a CMOS 3T-APS, see Section 1.3.2.

1.3 Technologies

The dominant image sensor technologies, CCD and CMOS, were born in the late 1960s and early 1970s, respectively. At the time, CMOSs performance was limited by available lithography technology and they suffered from large FPN caused by dark current nonuniformity, allowing CDDs to dominate for the next 25 years.

In the early 1990s there was a growing interest in CMOS image sensors because of the customer demand for miniaturized, low-power, and cost-effective imaging systems. The original argument for the renewal of CMOS image sensors as a competitor to CCD technology was generally based on several ideas: lithography and process control levels, integration capacity, lowered power consumption, reduced imaging system size, and the ability to use the same CMOS production lines. Additional arguments favouring CMOS included operation with a single power supply and the ability to do region-of-interest or windowing with the imagers. After a decade, the experience revealed the veracity under the previous premises. Integration and power dissipation are decisive advantages of CMOS technology, whereas CCD preserves a greater ability for cost-effective adaptation and performance.

Today, both CCDs and CMOSs dominate the image sensors industry in their own way taking advantage of the strengths and opportunities of both technologies. For instance, CCDs are used in digital cameras such as Single-Lens-Reflex (SLR) for good quality images and CMOSs are used in webcams and toys due to their low power consumption and compact size. Future CMOS image sensor technology development would yield good image quality with compact sized, low power sensors.

1.3.1 CCD image sensors

CCD technology prevailed since its invention in late 1960s because it provided better solutions to the typical problems such as FPN and it had a higher FF, smaller pixel size, larger format, etc, than CMOS, which could not compete with CCD performance. Although the research was mainly focused on CCD, this technology had also some limitations. For instance, CCDs have a high power consumption, suffer from blooming and smearing, need many different voltage levels and are sensitive to radiation. Furthermore, CCDs can not be monolithically integrated with analog readout and digital control electronics. In addition, CCD image sensors cannot guarantee their functionality over the whole temperature range or cover all lighting conditions

during daytime required by new applications. There is also a need to acquire images in a very short time for high speed applications, requiring short integration time.

CCD technology has undergone incremental advances in device design, materials and fabrication technology. CCD image sensors have steadily increased their QE and integration capacity, decreased the dark current and the pixel size, reduced operating voltages and improved signal handling. Consequently, CCDs now yield better performance with less power and reduced size. As a result, today CCD image sensors have a prominent role in high-volume uses, such as mobile phones, digital camera recorders and consumer digital cameras, as well as high-performance applications such as professional photography and industrial, scientific, medical and aerospace uses.

Implementation and operation

A CCD imager is an array of closely spaced MOS capacitors, which consist of a thin layer of oxide on top of a piece of semiconductor. The oxide is covered with a conductive material, often a metal or highly doped polysilicon.

Recording an image using a CCD imager comprises several processes: generation of charges by incident photons, collection of charges by the nearest potential well, transfer of charge packets through the CCD array, and readout by the output preamplifier. Firstly, the MOS structure is biased to a suitable voltage, leading to a space-charge region of a certain extent in the semiconductor. Then, photocharge is separated by the electric field and it is integrated on the MOS capacitance, collected at the interface between semiconductor and oxide. Finally, this signal has to be transported as efficiently as possible to an output amplifier, responsible for making this signal available to the on-chip electronics.

Charge is transferred from one capacitor to the next by controlling potential wells. In this way, the CCD acts as an analog shift register. Charge transfer must occur at high enough rate to avoid corruption by leakage, but slow enough to ensure high charge transfer efficiency. Therefore CCD requires that the space between electrodes be as narrow as possible and multi-polysilicon-layer overlapping electrodes (multi-phase driving) are used in general. Figure 1.6 represents an example of a three phase CCD and Figure 1.7 shows the corresponding timing diagram. During integration, t_1, a higher gate voltage V_{g1} is applied to gate 1 than to gates 2 and 3. This forces the material under gate 1 into deep depletion, so gate 1 serves as the signal charge collection and storage element. During t_2, the voltage applied to gate 2 is pulsed to a high level while maintaining the voltage applied to gate 1. Thus the stored charges

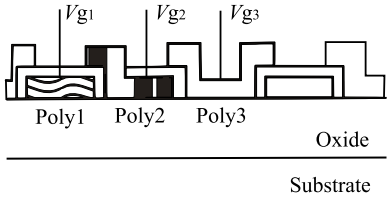


Figure 1.6: CCD stage with three polysilicon layers.

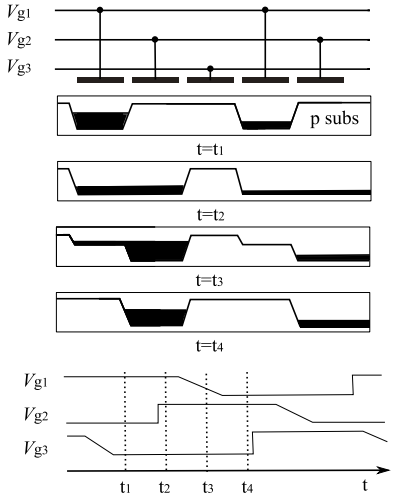


Figure 1.7: Charge transfer in CCD: potential wells and timing diagram.

are distributed into the potential wells under gate 1 and gate 2. In t_3, the voltage applied to gate 1 decreases slowly while maintaining the voltage applied to gate 2. Thereby, the charges initially stored under gate 1 are transferred into the potential well under gate 2, t_4. Consequently, after one cycle of the three-phase clock, the signal charge packet has been transferred to the next pixel. Repeating this process results in a linear motion of the charge packet from the original pixel to the end of the row where it is measured by generating either a voltage or current signal. An optical image represented by the stored charge packets is obtained by scanning through the CCD array.

Frame Transfer CCD (FTCCD)

Depending on the choice of pixel arrangement and interconnection in the array, different types of CCD image sensors result. Figure 1.8 is a block diagram of a Frame Transfer CCD (FTCCD), which consists of a light-sensitive area, a frame-store area, a horizontal charge transfer CCD, and an output circuitry. The light-sensitive area and the frame-store area are made up of a multichannel vertical transfer CCD, which transfers charge packets in parallel vertically. The frame-store area and the horizontal charge transfer CCD are covered by a light shield metal. The electrons generated in or near potential wells formed in the light-sensitive area are gathered and integrated in the potential wells as imaging signal charge packets. The signal charge packets integrated for a predetermined period are transferred in parallel toward the frame-store area, which acts as an analog frame memory. After this operation, the charge packets in a horizontal line are transferred into the horizontal charge transfer CCD and they are transferred to the output circuitry serially and output as voltage signals, one after another. The big advantage of the FTCCD is that the whole light-sensitive area is photosensitive and because FTCCD has a simple pixel structure, it is relatively easy to make a pixel size small, although it has the disadvantage of requiring extra charge frame-store area. However, the main disadvantage of the FTCCD principle is the after-exposure of bright areas that can occur when the photocharge pattern is transported from the light-sensitive area into the light-shielded charge frame-store area. This occurs because the light-sensitive area remains light-sensitive during the vertical photocharge transportation time. The after- exposure effect in FTCCDs can create saturated columns without any contrast information. For this reason, high-quality FTCCD cameras employ a mechanical shutter, shielding the light-sensitive area from incident light during the vertical photocharge transportation time.

Interline Transfer CCD (ITCCD)

In consumer applications, a mechanical shutter is impractical to use, and for this reason Interline Transfer CCD (ITCCD) principle is employed, Figure 1.9. Photocharge is collected in the individual pixels, and after the exposure time the photocharge is transferred via the pixels transfer register into a corresponding vertical CCD column. These CCD columns are shielded from light with an opaque metal layer. A two-dimensional photocharge distribution can therefore be shifted downwards, one row at a time, into the horizontal output register, from where the photocharge packets are read out sequentially. With the ITCCD principle there is essentially no time-constraint in exposing the pixels and transferring their accumulated photocharge

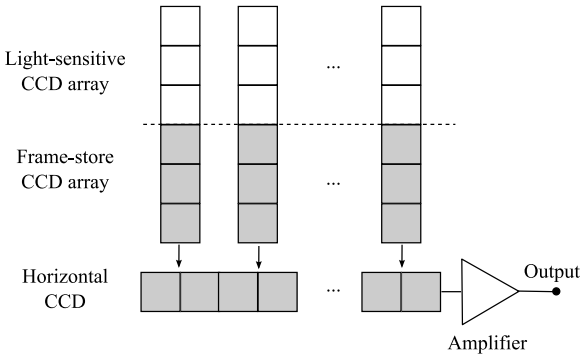


Figure 1.8: Frame Transfer CCD (FTCCD).

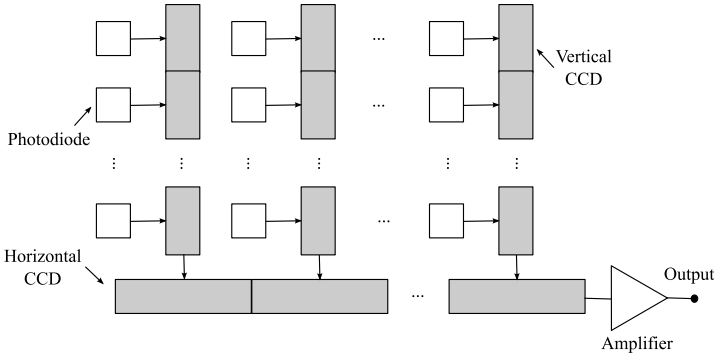


Figure 1.9: Interline Transfer CCD (ITCCD).

under the shielded columns. In addition, as the vertical CCD columns are shielded, the after-exposure problem is much less severe than in FTCCDs. On the contrary, the FF is reduced because the column light shields reduce the available photosensitive area on the image sensor surface. The desirable properties of the ITCCD make it the image sensor of choice for most of today's video and surveillance cameras, especially for consumer applications.

Field-Interline-Transfer CCD (FITCCD)

Although the column light shield in the ITCCD is an efficient light blocker, there is always some residual photocharge seeping into the columns from the sides. For this reason, an ITCCD can still show some after-exposure effects. For professional applications such

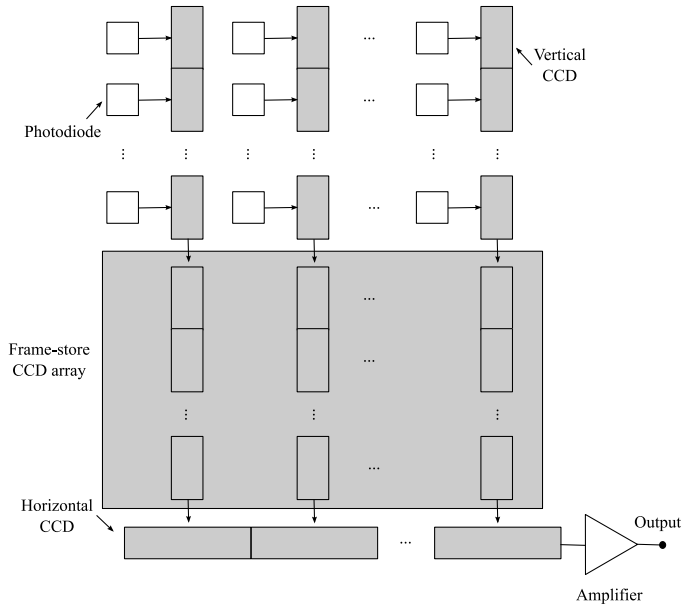


Figure 1.10: Field-Interline-Transfer CCD (FITCCD).

as video broadcasting, this is considered not acceptable, and a combination of FTCCD and ITCCD principles has been invented to overcome this problem, the Field-Interline-Transfer CCD (FITCCD), illustrated in Fig 1.10. The upper part of a FITCCD really consists of an ITCCD. The lower part, however, is like the frame-store area and horizontal charge transfer CCD of a FTCCD. The FITCCD is operated by acquiring an image conventionally, making use of the ITCCD variable exposure time functionality. The resulting two-dimensional photocharge distribution is then shifted quickly under the shielded vertical columns, from where it is transported very fast under the completely shielded intermediate storage register. The sequential row-by-row readout is then effectuated exactly as in FTCCDs.

1.3.2 CMOS image sensors

Although the first CMOS image sensors were developed in the 1960s, CMOS imagers did not begin to be a strong alternative to CCDs until early 1990s. Their most important feature was that they would satisfy the demand for low-power, miniaturised and cost-effective imaging

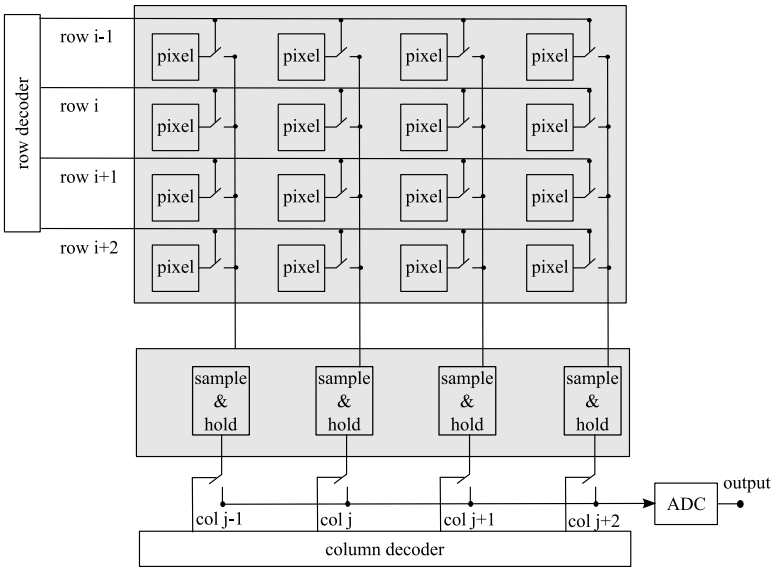


Figure 1.11: Overall CMOS image sensor architecture.

systems. Moreover, CMOS image sensors offered the possibility to monolithically integrate a significant amount of VLSI electronics on-chip and reduce component and packaging costs.

The improvement of CMOS image sensors has opened up new application areas and they can compete with CCDs in applications such as IR-vision. Besides this, there are many vision systems for X-ray, space, medical, 3D, consumer electronics, automotive or low-light applications which need highly integrated systems and can take advantage of the CMOS image sensors on-chip functionality. Furthermore, vision systems have to offer good imaging performance with low noise, no lag, no smear, good blooming control, random access, simple clocks and fast readout rates.

Implementation and operation

CMOS image sensors are mixed-signal circuits containing pixels, analog signal processors, analog-to-digital converters, reference voltage and bias generators, timing controller, drivers, digital logic and memory. The on-chip processor can implement basic image processing, such as exposure control, gain control, white balance, and colour interpolation. There are several

CMOS imager architectures depending on their purpose, but a general example can be seen in Figure 1.11.

The pixels in the array are addressed by a row and a column decoder. In fact, CMOS image sensors can be classified by how many pixels are simultaneously selected and processed. Firstly, in a pixel serial-processing architecture, only one pixel is selected at a time. Thus, the pixels are processed sequentially. Secondly, column parallel readout architecture is very popular and is used in most CMOS image sensors. Pixels in a row are selected simultaneously, stored in a line memory, and processed sequentially. Finally, pixel parallel, or frame simultaneous readout, is used for special applications, such as very high-speed image processing. It contains a processor element per pixel, which performs image processing in parallel. Then, the processed signal is read through the global processor.

CMOS image sensors can be also classified by the pixel architecture. Pixel circuits are mainly divided into Passive Pixel Sensors (PPSs) and Active Pixel Sensors (APSs) and the standard configurations are revised below.

Passive Pixel Sensor (PPS)

PPSs were the first CMOS image sensors and they are based on pixels without internal amplification. In these devices each pixel consists of a photodetector and a switching transistor in order to connect it to a readout structure, see Figure 1.12, in a similar way to a Dynamic Random Access Memory (DRAM). The row readout is done in two stages. First, the row is transferred to the column capacitors and then the column decoder is used to serially read out the pixel values. In spite of the small pixel size capability and a large FF, they suffer from low sensitivity and high noise due to the large column capacitance with respect to the pixel capacitance.

Active Pixel Sensor (APS)

APSs implement a buffer per pixel, Figure 1.13. This buffer is a simple source-follower and the column amplifier and decoder are identical to PPS. It is well known that the insertion of a buffer/amplifier into the pixel improves the performance of the pixel. Power dissipation is minimal and, generally, less than in CCDs, because each amplifier is only activated during readout. In addition, reading is not destructive and can be much faster than for PPS. Nevertheless, conventional APS suffer from a high level FPN due to wafer process variations that cause differences in the transistor thresholds and gain characteristics. A solution is to use a

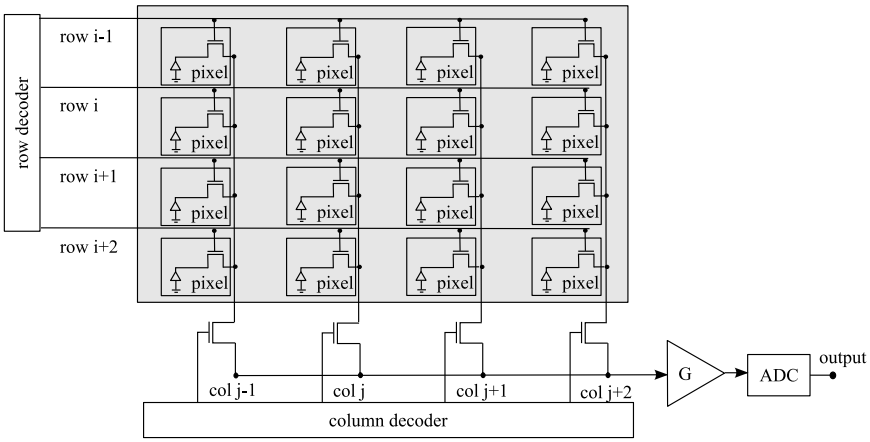


Figure 1.12: Passive Pixel Sensor (PPS) architecture.

correlated double sampling circuit, which can almost eliminate the threshold variations that cause offsets in the background.

Since many variations of APS configurations have been proposed, the most used structures are revised:

– Photodiode APS (PD APS or 3T-APS):

The photodiode APS depicted in Figure 1.14(a) is considered a standard and it was described by Noble in 1968 [63]. The operation of a 3T-APS is as follows. First, the reset transistor is turned on and the photodiode is reset to the value $V_{DD} - V_{TH}$, where V_{TH} is the threshold voltage of the reset transistor. Next, the reset is turned off and the photodiode is electrically floated. The photogenerated carriers are accumulated in the photodiode junction capacitance C_{PD} and they change the potential in the photodiode, V_{PD}, which decreases according to the input light intensity as [63]

$$\frac{dV_{PD}}{dt} = \frac{I_{ph}}{C_{PD}} \tag{1.28}$$

After an accumulation time, the select transistor is turned on and the output signal in the pixel is read out in the vertical output line. When the readout process is finished, the select transistor is turned off and reset is again turned on to repeat the above process.

As the drain of the reset transistor is connected to V_{DD}, the source terminal has to adequate its voltage level to obtain values of V_{DS} and V_{GS} which define a current through

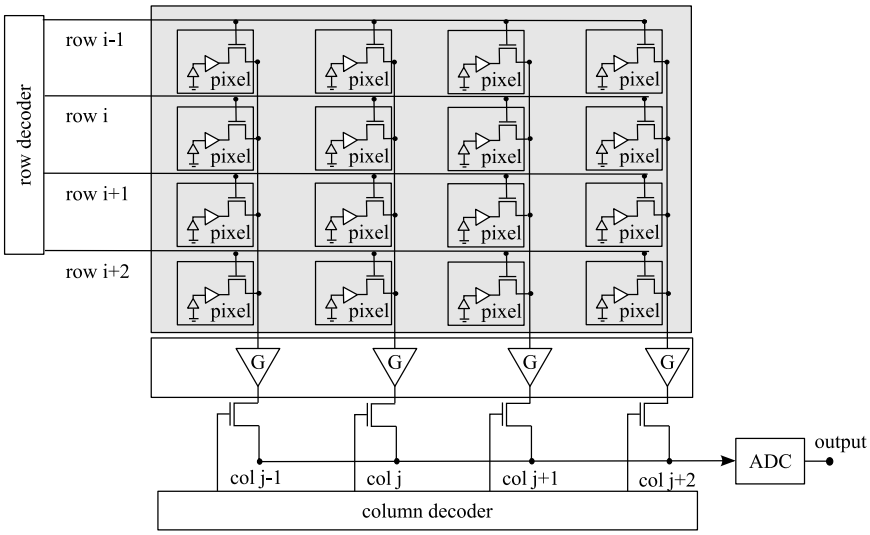
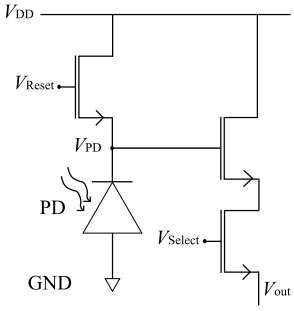


Figure 1.13: Active Pixel Sensor (APS) architecture.

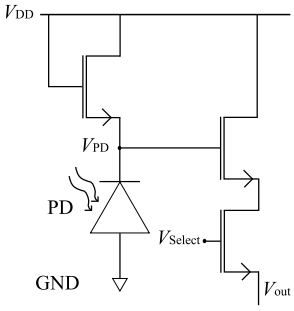
the transistor equal to the photocurrent. These values of the electrical potential difference tend to be small and the source voltage tends to V_{DD} because the photocurrent values are very low, specially for low light intensity. Thus, the signal at the gate of the reset transistor, V_{Reset}, determines its operation mode, and gives rise to the soft and hard reset definitions:

- Soft reset: if $V_{Reset} < V_{\mathrm{DD}} + V_{\mathrm{TH}} \Rightarrow V_{\mathrm{GS}} < V_{\mathrm{TH}}$ (subthreshold)
- Hard reset: if $V_{Reset} > V_{\mathrm{DD}} + V_{\mathrm{TH}} \Rightarrow V_{\mathrm{GS}} > V_{\mathrm{TH}}$ (above threshold)

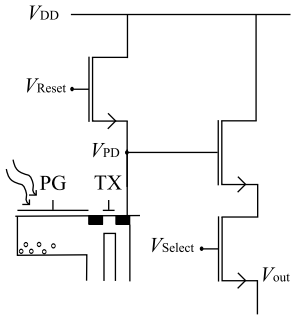
Although the 3T-APS overcomes the disadvantages of the PPS in terms of velocity and SNR, there are also several issues. It is difficult to suppress KTC noise and the photodiode design is constrained, as the photodiode acts simultaneously as a photodetection and photoconversion region. That is, the full-well capacity increases as the photodiode junction capacitance C_{PD} increases, while the conversion gain is inversely proportional to C_{PD}. This implies that the full-well capacity and the conversion gain have a trade-off relationship in a 3T-APS.



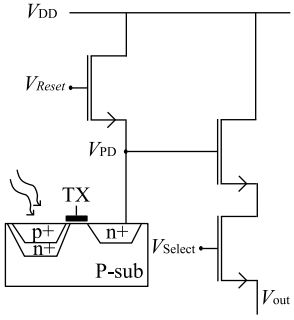
(a) 3T-APS schematic.



(b) Logarithmic APS schematic.



(c) Photogate APS schematic.



(d) Pinned photodiode schematic.

Figure 1.14: Different Active Pixel Sensor (APS) structures.

– Logarithmic APS:
The logarithmic APS configuration is very similar to 3T-APS, Figure 1.14(b), but the reset transistor is no longer used in a reset mode because its gate is connected to the drain voltage. The naturally linear photogenerated current is converted into a logarithmic voltage by means of the I–V characteristic of the reset transistor operating in subthreshold,

$$V_{PD} = V_{DD} - \frac{KT}{q} \ln\left(\frac{I_{ph}}{I_s}\right) \tag{1.29}$$

where I_s is the reverse-bias saturation current. A non-linear output permits a larger dynamic range but a smaller output voltage swing, leading to a low signal-to-noise ratio.

– Photogate APS (PG APS):
The photogate APS was introduced by the Jet Propulsion Laboratory in 1993 for high performance scientific imaging and low light applications [86]. A typical schematic is shown in Figure 1.14(c). It employs the operation principle of the CCD concerning integration, transport, and readout inside the pixel to reduce noise and enhance the quality of images. The photogate APS uses five transistors per pixel: a reset, a photogate (PG) to integrate the signal charge, a transfer gate (TX) to separate the PG from the output node, and a source-follower and a select transistor which have the same function as those in photodiode APS.

Before reading a row, the floating node is reset to $V_{\mathrm{DD}} - V_{\mathrm{TH}}$, where V_{TH} is the threshold voltage of the reset transistor. During integration, the photocharge is accumulated in the potential well under the photogate. To transfer the accumulated charge on the photogate to the floating node, the transfer gate is turned to an intermediate voltage $(< V_{\mathrm{DD}}/2)$ and the gate voltage is lowered to 0 V, like in CCD operation. The rest of the operation is identical to that of the photodiode APS.

The main advantage of the photogate APS is that the conversion gain is independent of the detector because the full-well capacity is determined by the voltage swing on the floating node and its capacitance. So most of the photosensitive area does not contribute to the charge to voltage conversion capacitance and the resulting large conversion gain allows for a high sensitivity. Nevertheless, a coupling diffusion needs to be inserted between the photogate and the transfer gate, which increases the effective floating capacitance during transfer resulting in lower conversion gain. The floating node capacitance is also very useful when performing correlated double sampling, which suppresses reset noise, 1/f noise, and FPN due to threshold voltage variations. A major benefit of photogate designs are their reduced noise features when operating at low light levels, as compared to photodiode sensors. However, the photogate APS presents lower FF and thus lower QE because it includes more transistors per pixel. In addition, the overlying gate material presents a low transparency.

– Pinned photodiode (PPD or 4T-APS):
The 4T-APS was developed as a detector with reduced dark current replacing the MOS varactor in CCDs [87], but it was proved to be equally beneficial for CMOS pixels to alleviate the issues with the 3T-APS. In a 4TAPS, the photodetection and photocon-

version regions are separated, analogous to the photogate APS. Thus, the accumulated photogenerated carriers are transferred to a floating diffusion (FD) where the carriers are converted to a voltage. The transfer gate transistor (TX) which is added to transfer the charge accumulated in the photodiode to the FD makes the total number of transistors in a pixel four, Figure 1.14(d) .

The 4T-APS basically consists of a p-n-p^+ structure where both p layers are on substrate potential (GND). As the voltage applied to the n-layer is increased, the depletion regions of both p-n junctions grow toward each other. At the so-called pinned voltage, the depletion regions meet and no more majority carriers can be extracted from the device as the device is fully depleted. The potential then remains fixed inside the device and cannot be increased any further. The light sensing operation is as follows. Firstly, the pinned photodiode is initially fully depleted. During the integration phase, photocarriers are stored in the depletion region, decreasing the potential of the photodiode below the pinned voltage. For readout, the floating diffusion FD is first reset to $V_{\mathrm{DD}} - V_{\mathrm{TH}}$ by turning on the reset transistor. This reset potential may now first be read out for correlated double sampling. Next, the transfer gate TG is opened and the complete photocharge is transferred to the FD, which ensures lag-free operation. The complete transfer takes place if the voltage on the FD remains above the pinning voltage while the photodiode operates below this voltage. A carefully designed potential profile can achieve a complete transfer of accumulated charge to the FD through the transfer gate. The rest of operation is identical to the photodiode APS.

The 4T-APS presents the same advantages than the photogate APS due to the location of the charge to voltage conversion node apart from the sensing area. Besides, the separation of the charge collection region away from the silicon surface into the bulk through the top p layer results in a great reduction of dark current. The 4T-APS has also much higher QE and less leakage currents and needs fewer control signals than the photogate APS. Despite their benefits, 4T-APSs have some drawbacks compared to 3T-APSs. The additional transistor reduces the FF, image lag may occur when the accumulated signal charge is not completely transferred into the floating diffusion, and it is difficult to establish fabrication process parameters for low noise and low image lag performance.

– Shared-pixel structures:
In recent years, novel APS pixel structures have arisen, which are designed to need less than three transistors per pixel. For instance, a configuration with 1.5 transistor per pixel is proposed in [12] and [16], where the amplifier circuit is shared by four pixels. In a similar way, 1.75 transistors per pixel structures are used in [81] and [15]. An example of the latter is depicted in Figure 1.15

1.3.3 CMOS vs. CCD

Many of the differences between CCD and CMOS image sensors arise from differences in their architecture, such as the signal transferring and readout methods. A CCD transfers the signal charge throughout the array to the output, converts it into voltage via a follower amplifier, and then serially reads it out. On the other hand, a CMOS image sensor converts the signal charge into a voltage signal at pixel-level and then the voltage signals are addressed using decoders. The main advantage of the CCD readout architecture is that it makes it possible to design image sensors with very small pixel sizes. Moreover, charge transfer is passive and therefore does not introduce temporal noise or FPN. By comparison, the random access readout of CMOS image sensors provides the potential for high-speed readout and window-of-interest operations at low power consumption. In addition, in high-speed operation the in-pixel amplification configuration gives better gain-bandwidth than a configuration with one amplifier on a chip. Even so, the in-pixel amplification may cause FPN and thus the quality of early CMOS image sensors was worse than that of CCDs. However, this problem has been drastically improved.

Other differences between CCD and CMOS image sensors arise from differences in their fabrication process technologies. CCDs are fabricated in specialized technologies solely optimized for imaging and charge transfer. Control over the fabrication technology also makes it possible to scale pixel size down without significant degradation in performance. However, the disadvantage of using such specialized technologies is the inability to integrate other camera functions on the same chip with the sensor. On the other hand, CMOS image sensors are fabricated in mostly standard mixed-signal processes and thus can be readily integrated with other analog and digital processing and control circuits. Although the recent development of CMOS image sensors may require dedicated fabrication process technologies, CMOS image

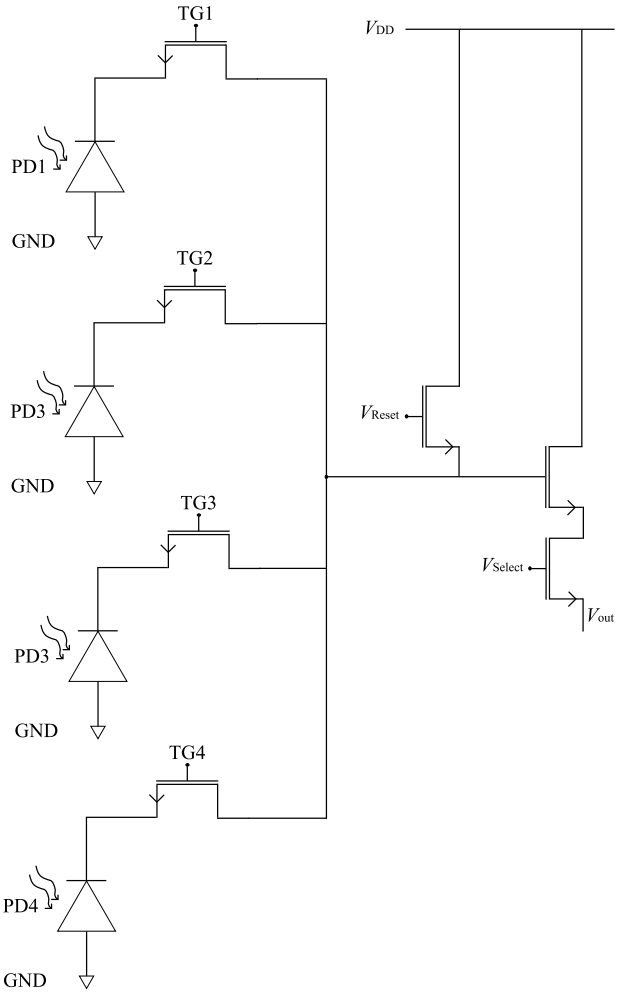


Figure 1.15: Shared-pixel structure: 1.75 transistors per pixel configuration.

CCD	CMOS
	Fabrication technology
Small pixel size	On-chip functionality
High fill factor	Readout flexibility
High sensitivity	Single power supply
High dynamic range	Low power consumption
Low noise	High-speed imaging
	No blooming and smearing effects

Table 1.2: Summary of the main advantages of CCD and CMOS image sensors.

sensors are still based on standard mixed-signal processes. Such integration further reduces imaging system power and size and enables the implementation of new sensor functionalities.

The main differences between CMOS and CCD image sensors are summarized in Table 1.2. As can be seen, each technology has its drawbacks as well as strong points aiming at different prospective markets. In the case of CMOS imagers their low cost, low power consumption, readout flexibility and on-chip functionality make them an ideal technology for consumer electronics products with an emphasis in high-resolution and small size as well as for dedicated applications such as ultra small cameras for medical imaging. In both cases, the size of the photosensing structure is a key factor in the overall sensor performance. The study of the impact of technology downscaling and the determination of the practical, as opposed to technological, limit on the photodiode size will be, therefore, the focus of this work.

1.4 Outline of the thesis

As explained above, CMOS technologies offer a wide range of opportunities for the fabrication of relatively inexpensive, low power and high resolution imagers with dedicated on-chip processing. Unfortunately, as a recent article in IEEE Spectrum pointed out, the metric most often used by camera manufacturers and marketers to advertise their products is the pixel count [88] and, while ensuring a certain resolution is necessary, there are a number of other factors which greatly influence the image quality such as the pixel and image sensor size, the quality of the embedded filters and microlenses or the camera lens itself. But, ultimately, it all centres on the individual pixels. In this sense, the goal of this work is the study of small photosensors in sub-micron CMOS technologies in order to assess the impact of technology scaling and the optimum photodiode size for enhanced sensitivity.

With this aim, the study of the photoresponse of the commonly used 3T-APS cell with p-n^+ and p-N_{well} junction photodiodes was considered. Specifically, a semianalytical model that takes into account the differences between the active area and the peripheral contributions in terms of the photodiode dimensions is presented in Chapter 2. Several functions to model the bottom and active area contributions were proposed and compared in order to take into account the physical phenomena which affect these devices in new technological nodes. With this aim in mind, two test chips, CHIP 1 and CHIP 2 described in Section 1.4.1, were fabricated in 180 nm CIS and 90 nm standard CMOS technologies.

The insight obtained from the semianalytical model suggested that for small photodiodes the largest active area not necessarily guarantees the highest response. To confirm this assumption a sub-pixel level study by means of a point source illumination was performed to analyze the behaviour of each region of the pixel in Chapter 3. To do so, an analytical model based on the solution of the steady-state equation in the different regions of the device was derived and validated with experimental data of p-n^+ and p-N_{well} junction photodiodes fabricated in a 90 nm standard CMOS technology, CHIP 2.

Once the importance of the lateral collection on the overall pixel response for small CMOS photodiodes was stated, the next step was the development of a compact, general and scalable model which can be easily extended to different photodiode sizes, geometries and technological nodes. This is done in Chapter 4, where the validation of the model with both simulated and experimental data is also shown. For the experimental characterization two test chips were fabricated in 180 nm and 65 nm standard technologies, CHIP 3 and CHIP 4 described in Section 1.4.1, respectively.

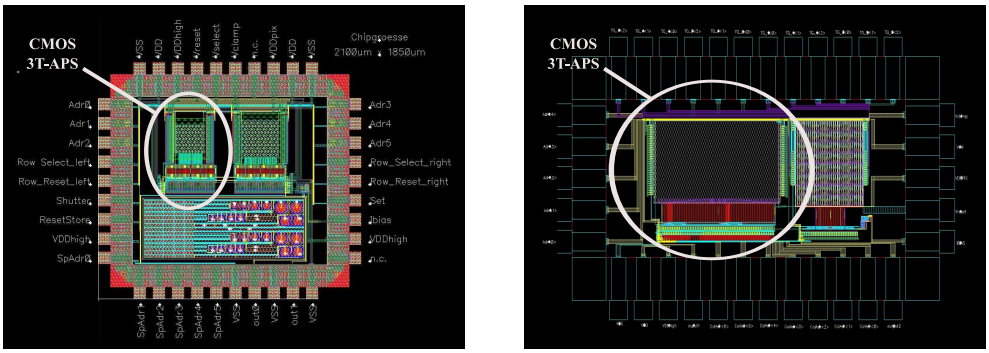
Finally, Chapter 5 contemplates the implementation of the aforementioned model in a hardware description language, particularly Verilog-AMS, in order to be used in Computer Aided Design (CAD) tools such as Cadence to aid the design process of CMOS imagers and permit the a priori optimization of the device performance.

1.4.1 CHIP 1 and CHIP 2: 3T-APS in 180 nm and 90 nm

Two different chips containing CMOS 3T-APS, called CHIP 1 and CHIP 2 from now on, were fabricated in UMC 180 nm CIS (CMOS Image Sensor) and UMC 90 nm standard technologies, respectively. The measurements and the results concerning these test arrays are considered in Chapter 2 and Chapter 3. The characteristics of these test structures are summarized in Table 1.3 and their layouts are described below.

	CHIP 1	CHIP 2
Technology	UMC 180 nm CIS	UMC 90 nm standard
Pixel size	3x6 μm^2	4x8 μm^2
Photodiode junction	p-n^+	p-N_{well}
Active area shape	octagonal	square

Table 1.3: Characteristics of CHIP 1 and CHIP 2.



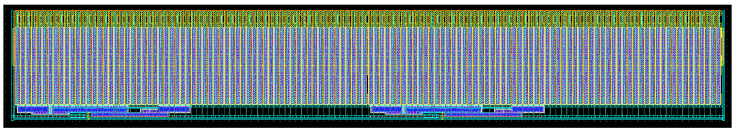
(a) Top layout of CHIP 1. (b) Top layout of CHIP 2.

Figure 1.16: Top layout of the test chips in UMC 180 nm CIS (left) and UMC 90 nm (right) standard technologies.

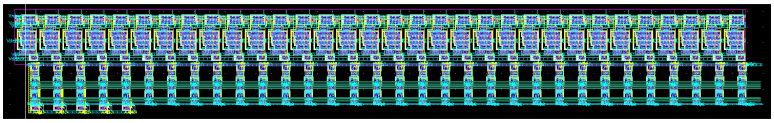
Figure 1.16 shows the top layout of both chips, where the location of the region of interest is specified. Both CHIP 1 and CHIP 2 consist of several sets of pixels with different sizes and geometries. The chips also include peripheral electronics to address the individual pixels such as a current source and row and column decoders, Figure 1.17, following the general scheme of a typical CMOS imager architecture, Figure 1.11.

Each array is composed of several subarrays of 8x16 identical pixels as it is shown in Figure 1.18, taken as an example. The pixel area consists of two functional parts: the photodiode itself and the 3T-APS electronics (reset, source follower, and row-select transistors to index the pixel and to read its value). In this design, the total pixel area is divided into two equal parts, one for the electronics (E) and the other one for the photodiode (PD), and the pixels are placed in a chessboard configuration, Figure 1.19. Figure 1.20 shows the layout of one pixel in each technology.

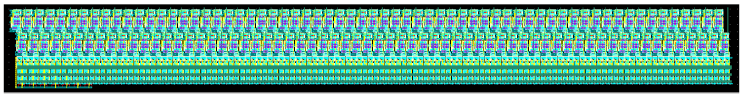
The electronics of the pixel has the same layout for all the pixels in the same technology, but photodiodes with different shapes and sizes were designed to study the geometrical effects.



(a) Current source.



(b) 5-to-32 row decoder.



(c) 7-to-128 column decoder.

Figure 1.17: Layout of the peripheral electronics surrounding the arrays of pixels in CHIP 2.

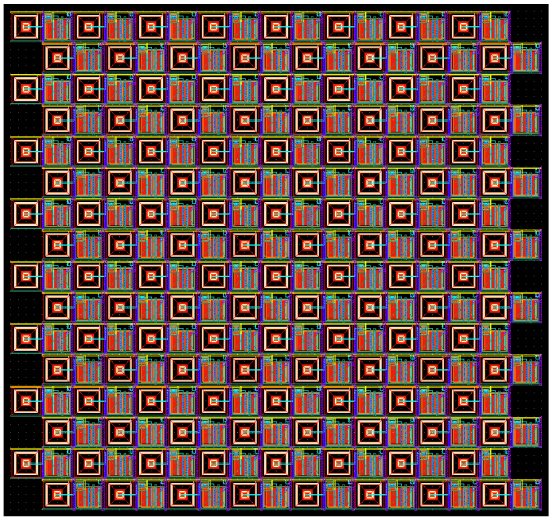
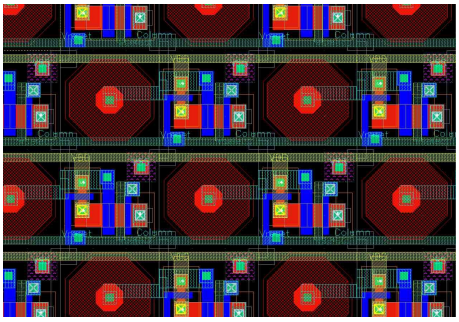


Figure 1.18: Layout of a subarray of 8x16 identical pixels in CHIP 2.

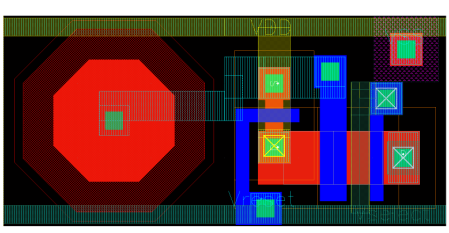
PD	E	PD	E	PD	E
	PD	E	PD	E	
PD	E	PD	E	PD	E
	PD	E	PD	E	
PD	E	PD	E	PD	E

(a) Schematic of the pixels arrangement.

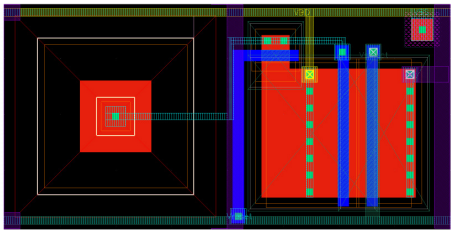


(b) Layout showing the pixels arrangement in CHIP 1.

Figure 1.19: Chessboard configuration of the arrays of pixels.



(a) Layout of a pixel in CHIP 1.



(b) Layout of a pixel in CHIP 2.

Figure 1.20: Layout of a pixel in UMC 180 nm CIS (left) and UMC 90 nm (right) standard technologies.

As an example, the layout of photodiodes with different geometries is shown in Figure 1.21 and Figure 1.22 for CHIP 1 and CHIP 2, respectively. It is important to note that the pixels in CIS technology include a colour filter array and a microlens layer. Moreover, a salicide blocking layer is included over the photodiodes in both technologies to protect the sensing area from salicide (self-aligned silicide). Salicide is used to get diffusion low ohmic for contacts but it also adds some dark current. Additionally, the photodiode area is prevented from metal and polysilicon coating.

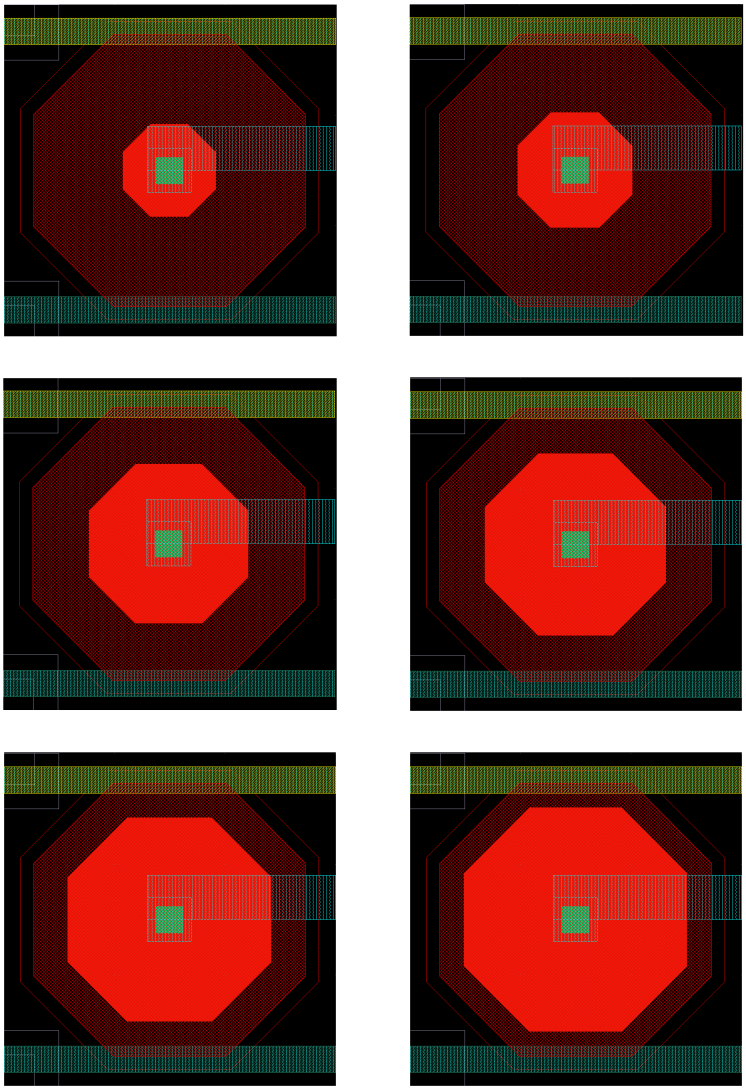


Figure 1.21: Layout of p-n$^+$ photodiodes with different diffusion areas in UMC 180 nm CIS technology.

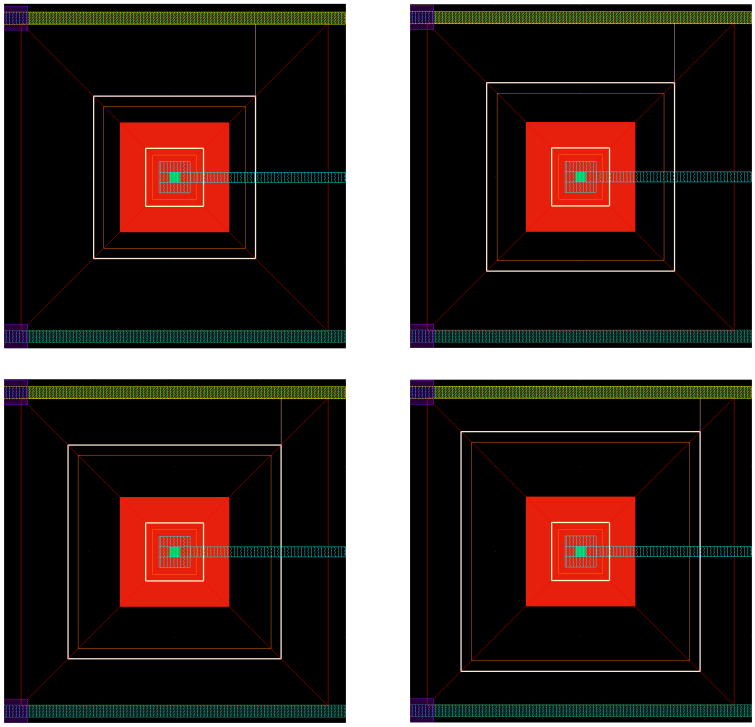
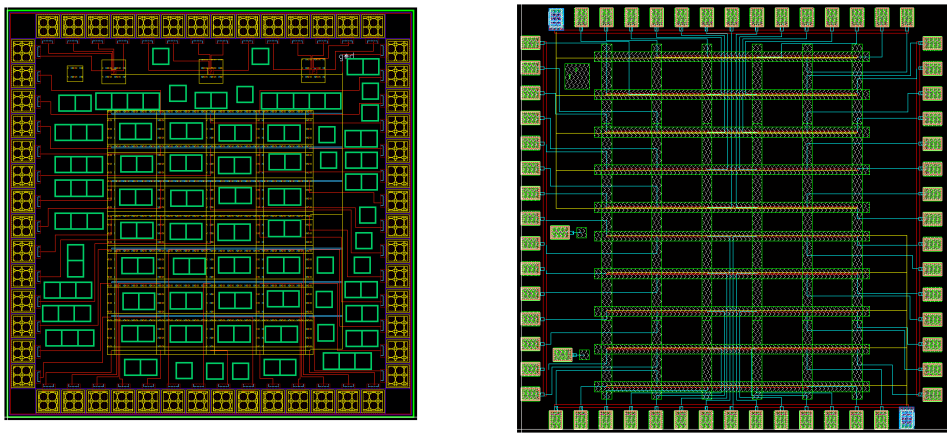


Figure 1.22: Layout of p-N_{well} photodiodes with the same diffusion area and different size of the well in UMC 90 nm standard technology.

1.4.2 CHIP 3 and CHIP 4: p-n^+ junctions in 180 nm and 65 nm

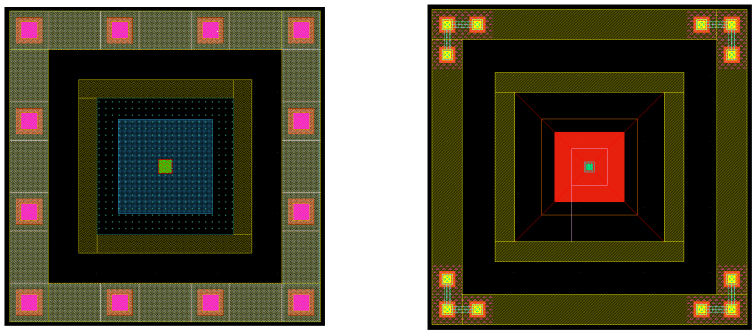
After a preliminary study of the pixel photoresponse as a function of the photodetector geometry, the thesis focuses on the modelling of p-n^+ photodiodes lateral photocurrent and the implementation of the model into a hardware description language. This part of the work is covered by Chapter 4 and Chapter 5. For this purpose, two chips called CHIP 3 and CHIP 4 containing isolated square p-n^+ photodiodes of different sizes were fabricated in AMS 180 nm and UMC 65 nm standard technologies, Figure 1.23. To characterize each device independently, each photodiode is directly connected to a raw pad without ESD protection in order to avoid unwanted coupling of capacitances to the sensing node.

An example of a photodiode layout in both technologies is depicted in Figure 1.24. A pair of metal rings are used to delimit the photodiode area and to ground the substrate by contacts,



(a) Top layout of CHIP 3. (b) Top layout of CHIP 4.

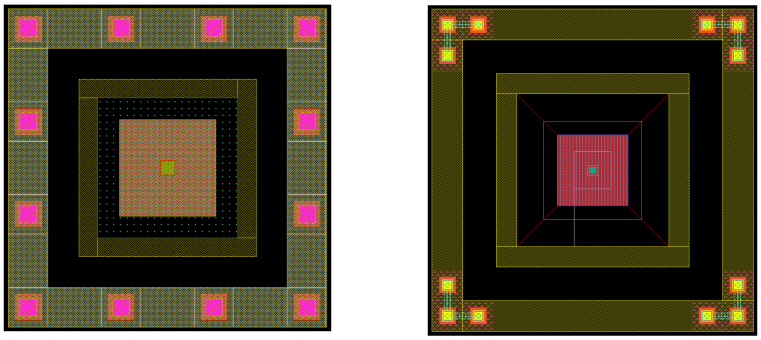
Figure 1.23: Top layout of the test chips in AMS 180 nm (left) and UMC 65 nm (right) standard technologies.



(a) Sample photodiode layout in CHIP 3. (b) Sample photodiode layout in CHIP 4.

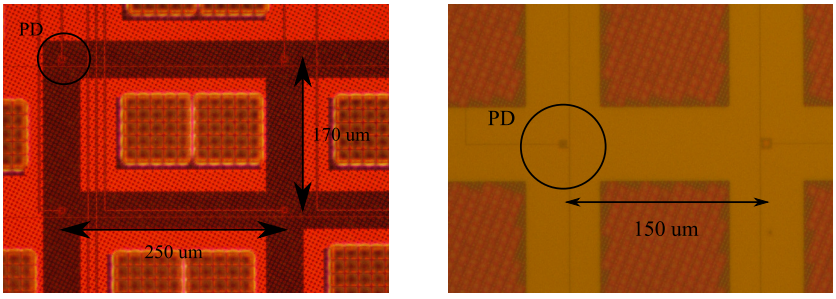
Figure 1.24: Photodiode layout including a substrate ground ring in AMS 180 nm and UMC 65 nm standard technologies.

respectively. In addition, two versions of each photodiode were designed and measured. The first one is used to characterize the photodiode under uniform illumination. The additional structure includes metal layers over the diffusion which block the penetration of light under this area, Figure 1.25. Consequently, the photoresponse due to the illumination of the sur-



(a) Sample photodiode layout in CHIP 3. (b) Sample photodiode layout in CHIP 4.

Figure 1.25: Photodiode layout including an optical shield over the diffusion in AMS 180 nm and UMC 65 nm standard technologies.



(a) Photodiodes in CHIP 3. (b) Photodiodes in CHIP 4.

Figure 1.26: Microphotographs of the isolated square p-n$^+$ photodiodes.

roundings of the photodiode can be characterized. In other words, these structures allow the measurement of the peripheral photocurrent. In both chips, all the sensing areas are protected from salicide, metal and polysilicon coating thanks to the appropriate blocking layers. Microphotographs of the photodiodes fabricated in both technologies are shown in Figure 1.26. As can be appreciated, they are widely spaced to be considered isolated structures.

CHAPTER 2

PHOTODIODE SEMIANALYTICAL MODEL

The principle of operation of a photodiode is based on the charge collection through the so-called active area, which is directly exposed to the light. However, photocarriers which are generated in the substrate within the device can be also successfully diffused to the junction. The depletion region of the junction is defined by its side-walls and bottom areas, which are responsible to the lateral and bottom collections, respectively. Thus, the so-called peripheral collection is the sum of the lateral and bottom collections. On the contrary, the crosstalk represents the photocurrent due to the carriers which are generated in the volume of a neighbouring device and are collected by the junction of interest. In the literature, peripheral collection, lateral collection, and crosstalk are sometimes used alike.

Although attention has been paid to the peripheral collection during the past decades, its effect can be neglected for large photodiodes. However, the emergence of new deep submicron technologies has motivated recent studies of the phenomena that govern the behaviour of these structures. Even though a three-dimensional treatment is the most suitable way to proceed, semianalytical approximations and experimental characterization are also very useful.

In 2006, a novel structure which showed the benefits of the peripheral utilization effect was presented, [89]. It consisted on a photodiode with circular holes opened on its diffusion area, which increased the total peripheral length. A test chip was designed, fabricated and tested in a 0.5 μm CMOS process. The results of several APS cells with 7, 11, 14 and 17 openings as well as a reference pixel demonstrated an improvement of the spectral response of the pixel. This study was extended in [30], showing that for the photodiode with 17 circular

openings under a 390 nm light source, the quantum efficiency and the pixel full-well capacity improved 12 % and 22 %, respectively, at the expense of doubling dark current compared with the reference pixel.

Although the work by S. U. Ay demonstrated the importance of peripheral collection, no efforts were made on mathematically quantifying its effect on the pixel photocurrent. The first semianalytical model of a CMOS pixel photoresponse including the peripheral collection was presented in [31], where an expression for the CMOS APS photosignal in terms of the geometrical shape and process data was derived. The model was compared with measurement results from a CMOS APS image sensor fabricated in a standard 0.5 μm CMOS process. The test chip included pixel sets of square, rectangular, circular, and L-shaped active areas of different sizes. Their response was analysed for different wavelengths in the visible range showing that longer wavelengths enabled better response. The model includes two fitting parameters that are wavelength dependent. It was found that there is a trade-off between the active area and the peripheral collection which results in an optimum photodiode active area size that enables the maximum photoresponse.

The previous model was used to predict the maximum pixel response in scalable CMOS technologies, [32]. The scaling influence on the device response depends on a large variety of parameters and an analytical expression determining the scaling trends has not been developed yet. The proposed approximation assumes that the ratio between the unity active area and the unity periphery contributions has a slight upward trend, mostly through the reduction of mobility and lifetime with increasing doping levels, and shrinkage of the depletion widths. A test array in a 0.35 μm CMOS process was measured to compare the experimental results and the theoretically predicted response, showing good agreement.

Later, another study of the peripheral photoresponse and crosstalk by the same authors was presented in [90]. Experimental measurements obtained by scanning several pixel topologies of CMOS APS in a standard 0.35 μm technology were performed using a sub-micron scanning system. The data include the pixel response and the crosstalk from each of the neighbours as a function of the photodiode dimension and wavelength exposure. The peripheral photoresponse was also studied by means of numerical device simulations using Medici^{TM} and based on the parameters of the technology employed for the test chip fabrication. A set of simulations for different values of the wavelength and distance between the depletion boundary and the illumination point were carried out to study the photocarrier concentration and its two-dimensional distribution. As different wavelength illuminations cause different

photocarrier distributions in the semiconductor depth, the original semianalytical model for the photoresponse estimation was enhanced by the separation of the lateral and bottom diffusion contributions. In addition, the improved model was applied to the crosstalk modelling and successfully compared with experimental measurements. However, no results in smaller technological nodes have been reported.

In this chapter, a semianalytical model based on [31, 32, 90] for the photoresponse estimation of 3T-APS with p-n^+ and p-N_{well} junction photodiodes in 180 nm and 90 nm technologies is reported. The aim of this approach is to take into account the physical phenomena which affect these devices in new technological nodes. Specifically, the model takes into account the differences between the active area and peripheral contributions in terms of the photodiode dimension. Several functions to model the bottom and the active area contributions are also proposed and compared. The model was tested with fabricated 3T-APS octagonal p-n^+ and square p-N_{well} junctions in UMC 180 nm CIS and 90 nm standard technologies, respectively, showing an accurate agreement with experimental data.

2.1 Test structures and experimental set-up

A p-n^+ and a p-N_{well} junction photodiode were modelled and tested in 180 nm and 90 nm technologies, respectively. Both structures have a n^+ diffusion which defines the active area, so called because it is the region of the surface most sensitive to the light. In both cases, the photodiode with the minimum active area which is allowed by the technology design rules is studied.

The geometrical shape of the photodiode active area is octagonal for the pixels in the 180 nm technology while those in 90 nm technology are square. A scheme of the pixel plan view and the parameters which define the active area in both technologies is shown in Figure 2.1, where E represents the electronics area. The total pixel area is 3×6 μm^2 and 4×8 μm^2 for 180 nm and 90 nm technologies, respectively. In the 180 nm technology, a represents the apothem of the octagonal active area, P its perimeter, A_t is the total area, and A the real value of the active area which does not take into account the contact and the metal areas over the diffusion which block the incident light. On the other hand, the pixels in 90 nm have an active area of $A_{diff} = l_{diff}^2$, where l_{diff} is the square side of the diffusion. However, the perimeter and total area are P and $A_t = l^2$, where l is the square side of the N_{well}. As with the pixels in 180 nm, the well area which is not covered by metal is represented by A. For each

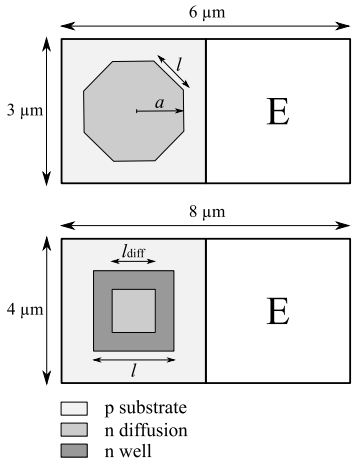


Figure 2.1: Pixel schemes with octagonal and square photodiodes.

a (µm)	P (µm)	A_t (µm^2)	A (µm^2)
0.42	2.78	0.58	0.28
0.52	3.45	0.90	0.54
0.72	4.77	1.72	1.27
0.82	5.43	2.23	1.74
0.92	6.10	2.80	2.28
1.01	6.69	3.38	2.82
1.05	6.96	3.65	3.07

Table 2.1: Parameters of the tested pixels in UMC 180 nm CIS technology.

value of l_{diff}, l takes different values between a maximum and a minimum value determined by the technology design rules. In Table 2.1 and Table 2.2, the fabricated and measured pixels in both technologies are summarized. More details about the layout of the test structures and readout system, CHIP 1 and CHIP 2, can be found in Section 1.4.1.

The pixels in the arrays were measured using a experimental set-up which consists of the following elements:

– a light source

– a DC voltage source to bias the chip

l_{diff} (μm)	l (μm)	A_{diff} (μm^2)	A_t (μm^2)	A (μm^2)
0.80	1.44	0.64	2.07	1.29
	1.78		3.17	2.36
	2.12		4.49	3.67
	2.46		6.05	5.21
	2.80		7.84	6.97
1.28	1.90	1.64	3.61	2.80
	2.20		4.84	4.01
	2.50		6.25	5.40
	2.80		7.84	6.97
1.52	2.08	2.31	4.33	3.50
	2.32		5.38	4.54
	2.56		6.55	5.70
	2.80		7.84	6.97
2.00	2.44	4.00	5.95	5.11
	2.56		6.55	5.70
	2.68		7.18	6.32
	2.80		7.84	6.97

Table 2.2: Parameters of the tested pixels in UMC 90 nm standard technology.

– a signal generator to generate the input pulses at the gate of the reset and the row-select transistors

– logic for the column and row selection

– an oscilloscope

Initially, some of the previous elements must be configured. The power of the light source is fixed, an adequate value of the DC voltage source is selected to bias the chip, and the reset and integration times are adjusted defining the appropriate input pulses at the gate of the reset and row-select transistors.

After the previous configuration, the pixels in the array are addressed and measured one by one. The reading of each pixel is a curve such as the one in Figure 2.2, taken as an example, where the reset and integration times are specified. The curve represents the output voltage versus time under particular illumination and bias conditions. The slope of this curve during the integration time represents the pixel photometric sensitivity in V/s lux, which is a measure of the pixel photoresponse, see Section 1.2.3. As it was described in Section 1.4, there is a

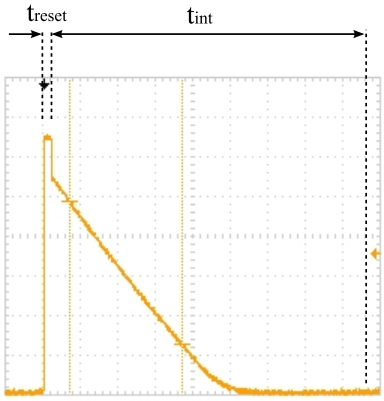


Figure 2.2: Output voltage curve of a pixel versus time.

subarray of identical pixels for each particular photodiode size, which provides a collection of curves for an appropriate statistical treatment.

2.2 Semianalytical model

Photon absorption in silicon depends mainly on the absorption coefficient α. This coefficient is a function of the wavelength in such a way that α increases when the wavelength decreases (Section 1.2.1). This means that the components of the light with shorter wavelengths are strongly absorbed in the first few micrometers of silicon, while the components with larger wavelengths are likely to generate photocarriers outside the depletion region. In this case, the photocarriers can be successfully diffused to the corresponding photodiode or to a nearby one (crosstalk), or they can be lost at a bulk recombination process. The successfully collected diffusion photocarriers through the bottom and the side-walls of the junction depletion region contribute to the total pixel photoresponse. This phenomenon is known as peripheral contribution. Peripheral contribution is the sum of the bottom and lateral diffusion contributions and, therefore, it depends strongly on the perimeter and area of the junction depletion region. Consequently, the total pixel photoresponse is the sum of the active area and the periphery contributions.

In this chapter, a semianalytical expression for the photoresponse estimation in terms of the photometric sensitivity is developed. The photometric sensitivity determines the output

signal of the image sensor illuminated by a certain light level within a specific integration time. This magnitude is the product of two terms: the conversion gain (CG) and the responsivity (R), see Section 1.2.3 and Section 1.2.4,

$$S = CG \times R \tag{2.1}$$

The conversion gain is inversely proportional to the total capacity of the photodiode, C_{PD},

$$CG = \frac{q}{C_{\mathrm{PD}}} \tag{2.2}$$

On the other hand, the responsivity measures the electrical output per optical input. As the photogenerated charges can be collected through the active and peripheral areas, the responsivity is modelled as the sum of two terms which take into account these two different contributions:

$$R = R_{\mathrm{A}} + R_{\mathrm{P}} \tag{2.3}$$

Thus the sensitivity, S, can be written as

$$S = q\frac{R_{\mathrm{A}} + R_{\mathrm{P}}}{C_{\mathrm{PD}}} \tag{2.4}$$

Since the goal is the study of the pixel photoresponse dependence on the pixel geometry, an alternative expression of Equation (2.4) in terms of active area or perimeter must be found, taking into account the physical meaning of the terms of the sensitivity.

2.2.1 Conversion gain

The photon conversion and charge storage element is a reverse-biased p-n junction diode. The total capacitance of the photodiode diffusion layer determines key pixel performance parameters. The junction area of the photodiode is controlled by the design, while peripheral junction depth and doping concentration are process and technology dependent.

In reverse-biased operation, the photodiode capacitance is defined as the depletion capacitance due to the majority carriers, which is the sum of the junction bottom area and junction side-wall capacitances. The diffusion capacitance due to the minority carriers only affects in forward-bias operation and, consequently, can be neglected. Therefore, the total capacity of the photodiode, C_{PD}, for both p-n^{+} and p-N_{well} depends on the unit junction bottom area capacitance (C_{A}) and unit junction side-wall capacitance (C_{P}) and it is given by Equation (1.18).

More details are given in Section 1.2.4 and the equation is copied below just for the sake of reader's convenience:

$$C_{PD} = C_A A + C_P A_P \tag{2.5}$$

where A and A_P are the photodiode junction and side-wall areas, respectively, and $A_P = Pd$, where d is the depletion region depth. Thus, the conversion gain is inversely proportional to the junction area and perimeter.

2.2.2 Responsivity: active area contribution, R_A

Regarding the responsivity, the geometrical and physical differences between p-n$^+$ and p-N$_{well}$ junctions must be considered. The first term, R_A, models the contribution of the photocarriers collected by the active area itself. This term is modelled as directly proportional to the active area for p-n$^+$ junctions,

$$R_A = C_1 A \tag{2.6}$$

However, p-N$_{well}$ junction photodiodes have a square diffusion with l_{diff} side and a square N$_{well}$ with $l > l_{diff}$ side. Although the diffusion defines the active area, the electron-hole pairs can also be generated in the well, albeit less successfully. In order to take this effect into account, different functions are considered to model this term for p-N$_{well}$ junction photodiodes.

Firstly, R_A is considered to be proportional to the diffusion area as was the case for p-n$^+$ photodiodes,

$$R_{A1} = C_1 A_{diff} \tag{2.7}$$

The main problem of this simplification was already mentioned. The carrier collection is underestimated because the photocarriers generated in the well surrounding the diffusion are not taken into account. This fact is expected to introduce a small error when the distance between the diffusion and the well is small in comparison with the diffusion size, but for a smaller diffusion area and a longer distance between the diffusion and the well the error is expected to be significant.

Another possibility is to model R_A as a term proportional to the well area,

$$R_{A2} = C_1 A \tag{2.8}$$

Using this approximation the photocurrent is overestimated. The error is more important for a high well area-to-diffusion area ratio because the model considers a contribution corresponding to a diffusion with the size of the well, but actually the collection of the well is not so high.

Given these considerations, the following function is considered, introducing a dependence on the diffusion area-to-well area ratio,

$$R_{\mathrm{A3}} = C_1 \frac{l_{\mathrm{diff}}}{l} A \tag{2.9}$$

As $\frac{l_{\mathrm{diff}}}{l}$ takes a value in the interval (0,1), this means that the responsivity of the active area is modelled to be directly proportional to the well area when $l \simeq l_{\mathrm{diff}}$.

Following the previous idea, the last function is proposed,

$$R_{\mathrm{A4}} = C_1 A^{l_{\mathrm{diff}}/l} \tag{2.10}$$

In this case, the responsivity is also proportional to the well area when the diffusion and the well have approximately the same size.

In all cases, C_1 has units of $\mathrm{e^-/s\,lux\,\mu m^2}$.

2.2.3 Responsivity: peripheral contribution, R_{P}

The second term of the responsivity, R_{P}, takes the peripheral diffusion current contribution (lateral and bottom contributions) into account, i.e., the photocarriers that are generated in the surroundings of the photodiode and are successfully diffused and collected by the photodiode, Figure 2.3 and Figure 2.4. It is assumed that this phenomenon depends mainly on:

(i) the bottom area and the side-walls of the junction depletion region,

(ii) the unoccupied photodiode surrounding area within the pixel,

(iii) the diffusion length of the photocarriers.

Consequently, R_{P} is considered to be proportional to the product of three terms, which represent the previous dependences,

$$R_{\mathrm{P}} = C_2 \cdot R_{\mathrm{P1}} \cdot R_{\mathrm{P2}} \cdot R_{\mathrm{P3}} \tag{2.11}$$

Next, how these terms were modelled is explained in detail.

The first term, R_{P1}, represents the influence of the peripheral area of the junction depletion region, both the bottom area and the side-walls, (i). The bottom area of the depletion region has approximately the same size as the photodiode active area, A. A function of this

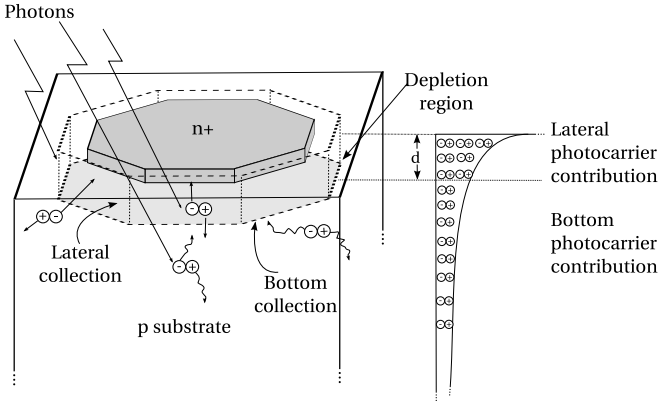


Figure 2.3: Diagram of the octagonal p-n^+ junction photodiode.

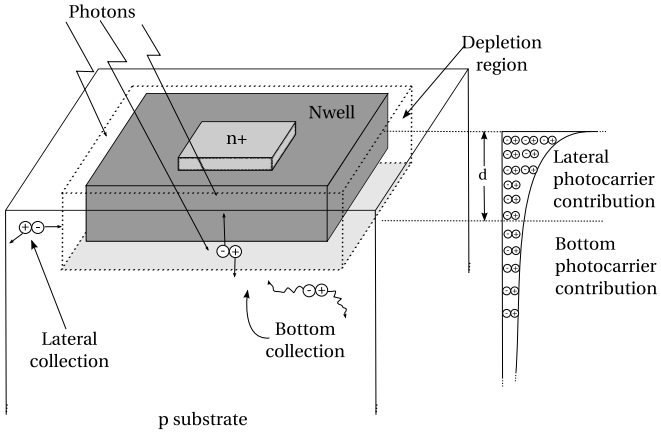


Figure 2.4: Diagram of the square p-N_{well} junction photodiode.

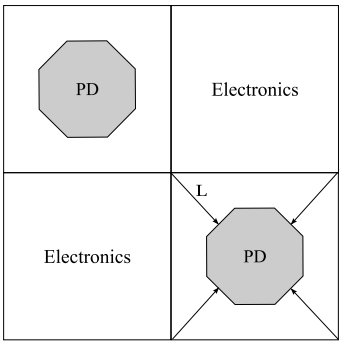


Figure 2.5: Different lateral contribution of the depletion region side-walls.

area, $f(A)$, is proposed to model its importance in the overall photoresponse. Two different expressions were chosen for this purpose which take a value between 0 and A:

$$f_1 = C \cdot A, \qquad 0 \leq C \leq 1 \tag{2.12}$$

$$f_2 = \log_{10}\left(1 + \frac{\ell}{L_{\text{diff}}}\right) A, \qquad 0 \leq \frac{\ell}{L_{\text{diff}}} \leq 9 \tag{2.13}$$

where ℓ represents the apothem (a) or the half square side ($l/2$) of the active area for octagonal and square photodiodes, respectively. The argument of the logarithm in f_2 guarantees that it takes a value between 0 and 1 because higher values would involve too large active areas which are out of the scope of this study. On the one hand, f_1 models the bottom area dependence as a fixed percentage of the bottom area independently of the junction size. On the other hand, f_2 is a function that takes into account the size of the photodiode and the diffusion length of the photocarriers (L_{diff}) to describe the following situations:

- When $\ell << L_{\text{diff}}$, the bottom contribution is not important because there are not many photocarriers susceptible to be captured by the bottom surface.
- When $\ell \simeq L_{\text{diff}}$, the bottom contribution becomes significant.
- When $\ell >> L_{\text{diff}}$, the peripheral contribution is directly proportional to the bottom area.

Regarding the side-walls and according to the particular pixel array arrangement, four lateral collecting surfaces of the depletion region (north, south, east and west directions) are

opposite some electronics region for the octagonal p-n^+ photodiodes, Figure 2.5. Since the microlens layer focus the light on the photodiode region, it is unlikely that these side-walls collect diffused photocarriers coming from the border with an electronics region and therefore their contribution is neglected in this analysis. However, the other four lateral collecting surfaces are opposite other photodiode regions, where the number of generated photocarries is higher. Therefore, the area of these four lateral collecting surfaces is considered,

$$\frac{A_{\mathrm{P}}}{2} = \frac{Pd}{2} = 4ld \tag{2.14}$$

and the contribution of the rest is not taken into consideration for octagonal p-n^+ photodiodes. On the contrary, there is not microlens layer for the square p-N_{well} photodiodes in the standard 90 nm technology, so the four side-walls are considered,

$$A_{\mathrm{P}} = Pd = 4ld \tag{2.15}$$

Thus, the influence of the bottom area and the side-walls of the junction depletion region is modelled as

$$R_{\mathrm{P1}} = (f + 4ld) \tag{2.16}$$

Secondly, another term must represent the fact that as the active area increases, the diffusion current contribution decreases and vice versa (ii). That is, the larger the diffusion the smaller the surrounding area where additional photocarriers can be generated. Consequently, this term is modelled as the ratio of the unoccupied photodiode surroundings area within the pixel to the total pixel area, A_{pix},

$$R_{\mathrm{P2}} = \left(\frac{A_{\mathrm{pix}} - A}{A_{\mathrm{pix}}}\right) \tag{2.17}$$

Finally, the third term of the peripheral collection, R_{P3}, describes the role played by the diffusion length of the photocarriers created within the substrate surrounding the photodiode, (iii). Being L the maximum diffusion distance between the depletion region and the corners of the photodiode region, Figure 2.5, this term reflects the fact that:

- If $L << L_{\mathrm{diff}}$, the probability of diffusion is high.
- If $L \simeq L_{\mathrm{diff}}$, the probability of diffusion is low.
- If $L >> L_{\mathrm{diff}}$, the contribution is negative, i.e., there are lost generated photocarriers.

Therefore this term is modelled as

$$R_{\mathrm{P3}} = \left(\frac{L_{\mathrm{diff}} - L}{L_{\mathrm{diff}}} \right) \tag{2.18}$$

Consequently, the achieved expression for R_P is

$$R_{\mathrm{P}} = C_2 \left(f + 4ld \right) \left(\frac{A_{\mathrm{pix}} - A}{A_{\mathrm{pix}}} \right) \left(\frac{L_{\mathrm{diff}} - L}{L_{\mathrm{diff}}} \right) \tag{2.19}$$

where C_2 has units of $\mathrm{e^-/s\,lux\,\mu m^2}$.

To conclude, the photoresponse model as a function of the photodiode dimension is

$$S = q \frac{C_1 A + C_2 \left(f + \frac{Pd}{2} \right) \left(\frac{A_{\mathrm{pix}} - A}{A_{\mathrm{pix}}} \right) \left(\frac{L_{\mathrm{diff}} - L}{L_{\mathrm{diff}}} \right)}{C_{\mathrm{A}} A + C_{\mathrm{P}} Pd} \tag{2.20}$$

for p-$\mathrm{n^+}$ photodiodes and

$$S = q \frac{R_{\mathrm{A}} + C_2 (f + Pd) \left(\frac{A_{\mathrm{pix}} - A}{A_{\mathrm{pix}}} \right) \left(\frac{L_{\mathrm{diff}} - L}{L_{\mathrm{diff}}} \right)}{C_{\mathrm{A}} A + C_{\mathrm{P}} Pd} \tag{2.21}$$

for p-$\mathrm{N_{well}}$ photodiodes, where f equals f_1 or f_2 and R_{A} equals R_{A1}, R_{A2}, R_{A3} or R_{A4}.

2.3 Results

The arrays of pixels with octagonal p-$\mathrm{n^+}$ and square p-$\mathrm{N_{well}}$ junction photodiodes in UMC 180 nm CIS and 90 nm standard technologies described in Section 2.1 were measured in terms of sensitivity in collaboration with the Fraunhofer Institute for Integrated Circuits IIS in Erlangen.

2.3.1 p-$\mathrm{n^+}$ photodiodes

The pixels with octagonal p-$\mathrm{n^+}$ photodiodes in UMC 180 nm CIS technology, Table 2.1, were measured under uniform white illumination conditions with an intensity of 40 lux. The curves given by the model in Equation (2.20) with $f = f_1$ and $f = f_2$ are depicted in Figure 2.6 and Figure 2.7, respectively, along with the experimental data marked with circles. The values used for the model parameters are given in Table B.1.

Both f_1 and f_2 fit the experimental data with high accuracy, as it is shown in terms of the coefficient of multiple determination, R^2, in Table B.3. Nevertheless, $f_1 = A$ gives the

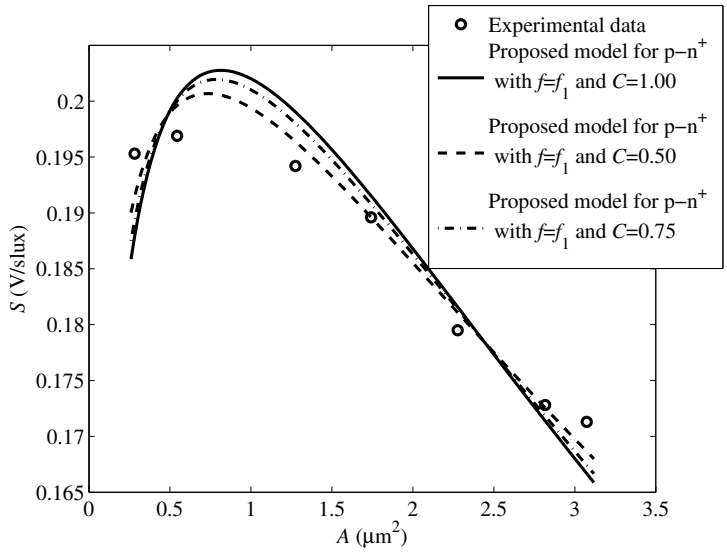


Figure 2.6: Sensitivity of the pixel with respect to the size of the p-n$^+$ photodiode in UMC 180 nm CIS technology. Experimental data (markers) are compared to the proposed model in Equation (2.20) (line) using $f = f_1$.

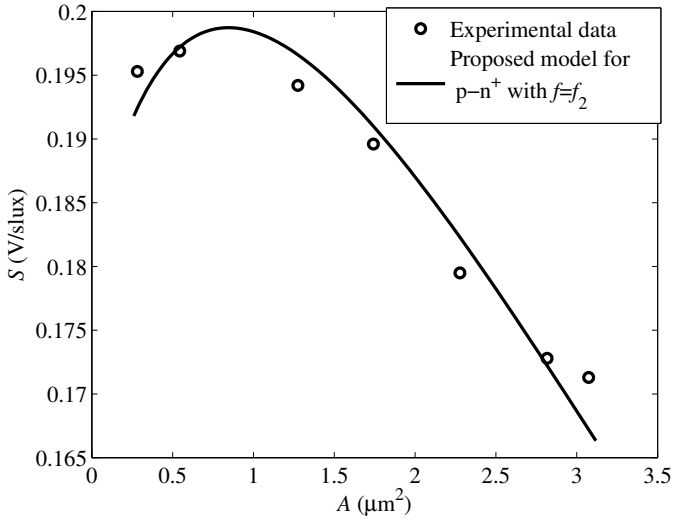


Figure 2.7: Sensitivity of the pixel with respect to the size of the p-n$^+$ photodiode in UMC 180 nm CIS technology. Experimental data (markers) are compared to the proposed model in Equation (2.20) (line) using $f = f_2$.

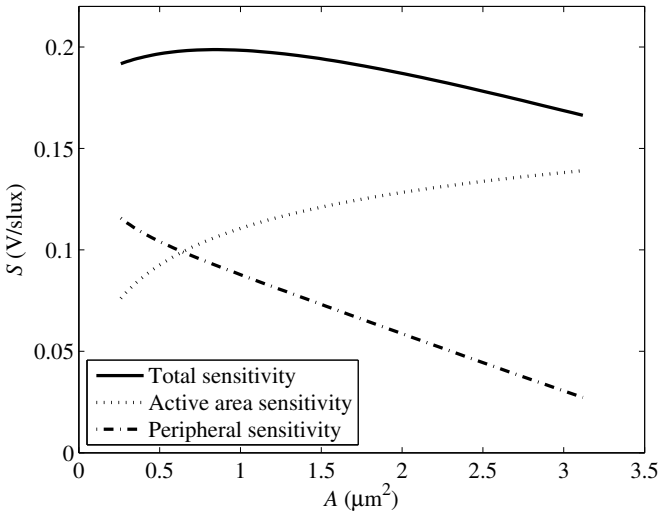
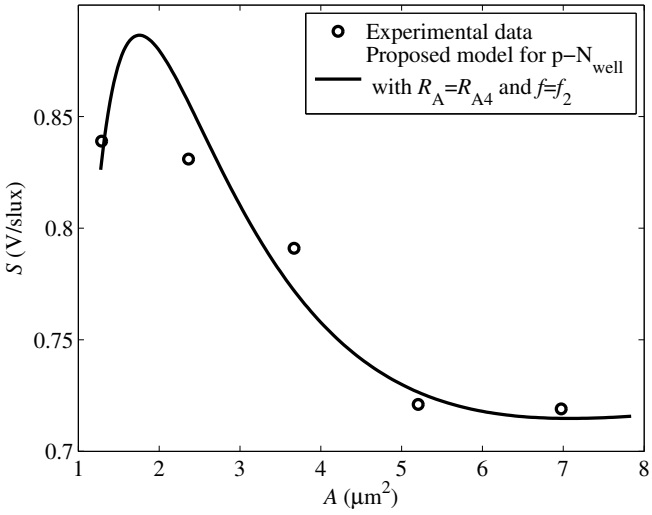


Figure 2.8: Sensitivity of the pixel with respect to the size of the p-n$^+$ photodiode in UMC 180 nm CIS technology given by the proposed model in Equation (2.20) using $f = f_2$. Active area and peripheral contributions are given separately.

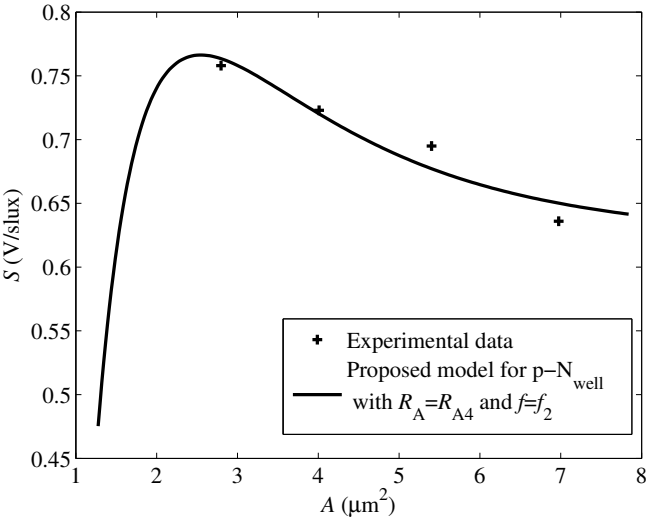
worst result, which suggests that a function to model the importance of the bottom area in the peripheral collection is desirable. Moreover, this function should be easily adaptable to other technologies and pixels. The function f_2 fulfils these requirements and it actually gives the best fit.

The main result that arises from both the measurements and the model is that the pixel photoresponse presents a maximum for a particular value of the photodiode active area. Increasing the diffusion beyond this point does not improve the overall performance as it compromises the peripheral contribution due to the reduction of the photodiode surrounding area. This suggests that, for small photodiodes in advanced CMOS processes, there is a trade-off between photodiode active area and peripheral contributions that must be taken into account in the design process in order to obtain the maximum photoresponse with the minimum area consumption.

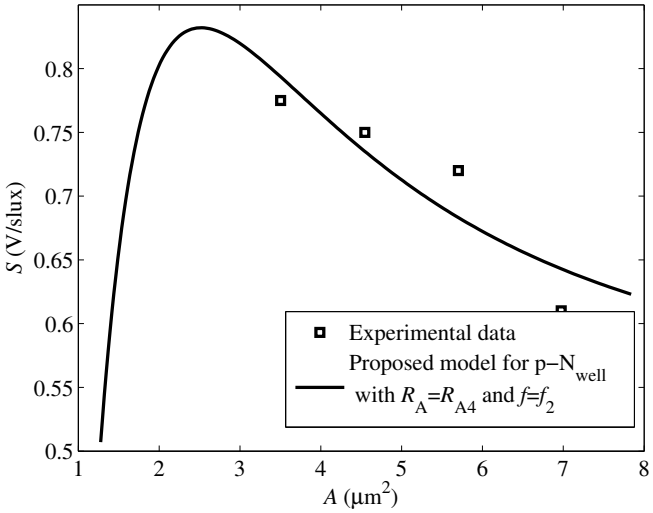
To corroborate this point, Figure 2.8 shows the active area and the peripheral contributions to the pixel sensitivity separately, i.e., the contribution of the photocarriers collected by the photodiode itself and the photocarriers that are generated in its surroundings and are success-



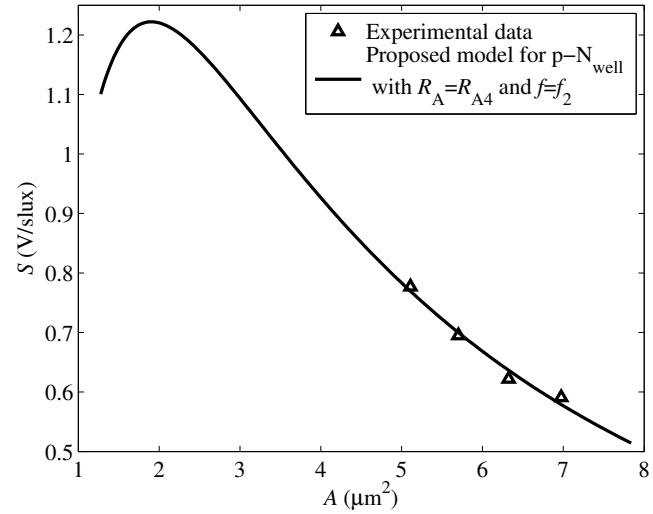
(a) $l_{diff} = 0.80$ μm.



(b) $l_{diff} = 1.28$ μm.



(c) $l_{\text{diff}} = 1.52$ μm.



(d) $l_{\text{diff}} = 2.00$ μm.

Figure 2.9: Comparison of the measured sensitivity of the pixels with respect to the size of the p-N_{well} photodiode in UMC 90 nm standard technology with the proposed model in Equation (2.21) using $R_A = R_{A4}$ and $f = f_2$.

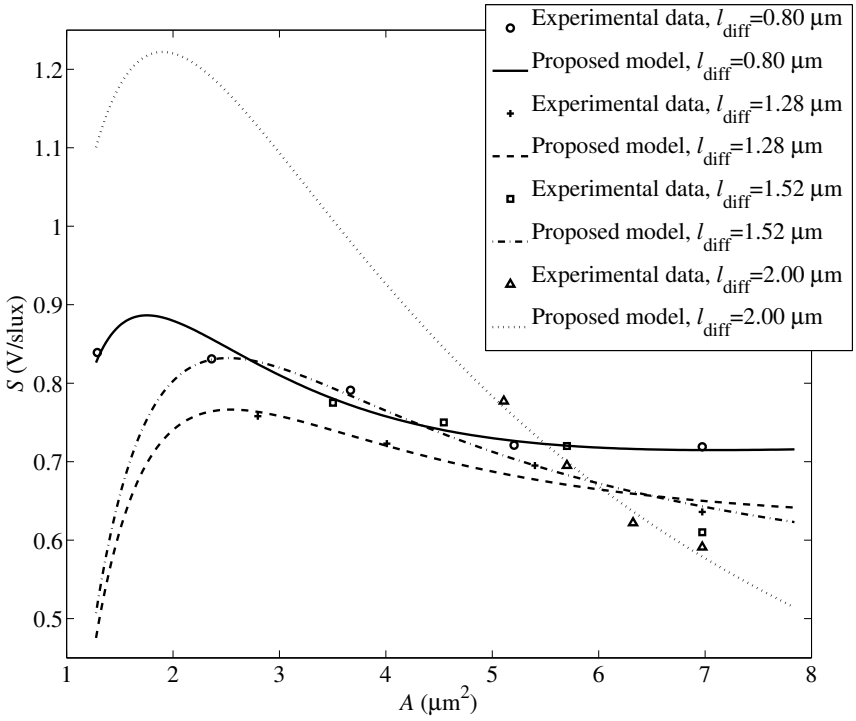


Figure 2.10: Comparison of the measured sensitivity of the pixels with respect to the size of the p-N_{well} photodiode in UMC 90 nm standard technology with the proposed model in Equation (2.21) using $R_A = R_{A4}$ and $f = f_2$ for different sizes of the diffusion area.

fully diffused and collected by the photodiode. It can be seen that the peripheral contribution increases as the diffusion area decreases, unlike the active area contribution, giving a maximum response for an optimum photodiode geometry corresponding to the intersection of both curves.

2.3.2 p-N_{well} photodiodes

The pixels with square p-N_{well} photodiodes in UMC 90 nm standard technology, Table 2.2, were measured under uniform 14 Klux 550 nm light source. The experimental data for each subset of pixels with the same diffusion area but different sizes of the well are plotted from

Figure 2.9(a) to Figure 2.8(d) marked with circles. Regarding the proposed model, the use of the function $f = f_2$, which models the relevance of the bottom area, was justified by the previous results. Besides, it was found by means of the coefficient of multiple determination, R^2, that a function R_A which takes into account the diffusion-to-well ratio is needed, specially for photodiodes with a small diffusion. A summary of the R^2 values for each curve can be found in Table B.4 to Table B.7. The fitting curves given by Equation (2.21) with $f = f_2$ and $R_A = R_{A4}$ are shown in Figure 2.9. The values used for the model parameters can be found in Table B.2.Despite none of the measured data sets present a clear maximum, Figure 2.9, the proposed model predicts an optimum photoresponse for a particular well area regardless of the diffusion area. The same result was found for p-n^+ photodiodes and demonstrated with experimental data. For the p-N_{well} junctions, the device dimensions corresponding with the maximum photoresponse predicted by the model are in the limit of the photodiode sizes permitted by the technology design rules constraints.

2.4 Conclusions

A semianalytical model for the photoresponse estimation of 3T-APSs with p-n^+ and p-N_{well} photodiodes was proposed. Specifically, the sensitivities due to the active area and peripheral collections were modelled separately. The responsivity due to the active area for p-N_{well} junctions takes into account both the diffusion and well areas. Moreover, different functions were proposed to model the collection through the junction bottom area. As a result, an expression in terms of the technology parameters and pixel geometry was found.

The model was successfully fitted with experimental measurements in UMC 180 nm CIS and UMC 90 nm standard technologies. It predicts a maximum response in terms of the junction size, which means that there is a trade-off between active area and peripheral contributions.

In conclusion, the peripheral response must be no longer neglected in sub-micron technologies and behavioural models taking into account its contribution are needed. In order to gain an in-depth understanding of these phenomena, a sub-pixel study of the photoresponse of the pixel by means of a point source illumination is presented in Chapter 3.

CHAPTER 3

PHOTODIODE ANALYTICAL MODEL: POINT SOURCE ILLUMINATION

The results of the previous chapter demonstrate that the traditional approach to the pixel design should be challenged when small photodetectors and advanced technologies are involved. For a particular pixel size, the largest active area no longer guarantees the highest response. Despite the fact that there are many studies about experimental characterization and comparison of different CMOS pixel cells, this procedure is not cost-effective and the prediction of the pixel photoresponse prior to manufacture becomes more important than ever. For this purpose, behavioural models for the photodetector considering both peripheral and active area collections are needed. In order to develop a photocurrent model for p-n junctions, a sub-pixel level study by means of a point source illumination is used to analyze the behaviour of each region of the pixel separately.

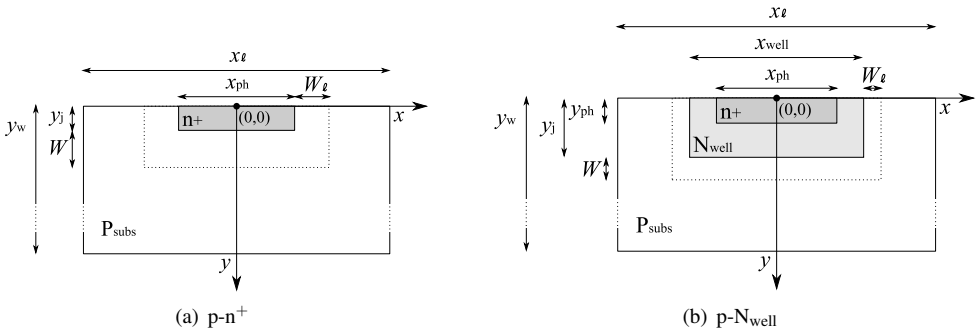
Despite the research on pixel size and shape and even some semianalytical models of the pixel photoresponse as a function of the active area size, there is a lack of studies at sub-pixel level. In fact, these measurements require a sophisticated optical equipment and take a long time to be carried out properly. Some of the first sub-pixel phoresponse maps were presented in [37] and were taken using a focused He-Ne laser scanning device with a beam diameter and a step size of approximately 1.5 μm and 2 μm, respectively. Despite the age of the technology and the pixels size this work is worth mentioning because of the methodology used. Measurements of N_{well} and P_{well} photogates fabricated in a 2 μm CMOS technology under a 632.8 nm and 488 nm laser beam were compared showing a higher response and

crosstalk in the N_{well}. Furthermore, the response dropped off more gradually at the edges of the N_{well} photogate area and increased for longer wavelength for both structures.

More recent measurements are found in [38], although the technological node is old as well. In this work, the Point Spread Function (PSF) was obtained experimentally via sub-pixel scanning. The PSF describes the response of an imaging system to a point source illumination, and the measurements were used to calculate the Modulation Transfer Function (MTF) for different pixel designs fabricated in a HP 1.2 μm process. Theoretical MTF derivation for those pixels was also presented, showing agreement with the experimental results. The same measurements were considered in [91] to fit a more comprehensive model which takes into account the effect of the minority carrier diffusion together with the effect of the pixel active area shape on the overall MTF. The diffusion length of the minority carrier was extracted and used for the creation of a two-dimensional symmetrical kernel matrix. The convolution of this matrix with the one representing the pure geometrical active area shape produced the desired unified PSF model.

The spot scan photoresponse was also used in the study of infrared detectors. A two-dimensional model for the photoresponse of HgCdTe n^+-p diffusion-limited diodes in the backside illuminated configuration was compared with the experimental and simulation data in [40]. In this work, an experimental and theoretical study of crosstalk between the nearest neighbour devices within a backside illuminated linear HgCdTe photovoltaic infrared sensing array was carried out. To measure crosstalk, a scanning laser microscope was used to obtain a spatial map of spot scan photoresponse at a temperature of 80K for individual p-on-n photovoltaic devices within the linear array. The experimental results were compared to simulations performed on a commercial two-dimensional device simulation package. The crosstalk measurements and simulations included results on mid-wavelength infrared planar device structures, as well as long-wavelength infrared mesa-isolated devices.

Consequently, there is a shortage of studies at sub-pixel level for silicon-based visible photodetectors in sub-micron technologies. In this chapter, an analytical model for p-n junctions under a point source illumination is presented. The model is derived from the solution of the steady-state continuity equation in the different regions of the device. Besides, experimental data corresponding to the output current of p-n^+ and p-N_{well} junction photodiodes fabricated in a standard UMC 90 nm technology are used to validate the accuracy of the model.



(a) p-n$^+$ (b) p-N$_{well}$

Figure 3.1: Photodiode structures.

3.1 Test structures and experimental set-up

A test array of CMOS 3T-APS with square p-n$^+$ and p-N$_{well}$ junction photodiodes in UMC 90 nm standard technology was characterized. The total pixel area is 4x8 μm^2 and the pixels are placed in a chessboard configuration. A detailed description of the test structure, CHIP 2, can be found in Section 1.4.1.

Figure 3.1 shows the modelled pixel photosensitive area cross sections for the p-n$^+$, Figure 3.1(a), and p-N$_{well}$, Figure 3.1(b). They consist of reverse biased p-n$^+$ and p-N$_{well}$ junction photodiodes with junction depth y_j and thickness y_w. The n$^+$ diffusion and the device are x_{ph} and x_ℓ wide, respectively. Diffusion depth and well width for the p-N$_{well}$ junction are y_{ph} and x_{well}. In reverse-bias operation three main regions are distinguished in the device: two quasi-neutral regions and the depletion region with thickness W (in y-direction) and W_ℓ (in x-direction). It is assumed that the depletion region is mainly located in the substrate because diffusion concentration is higher than substrate concentration.

The aim of these measurements is to obtain a pixel characterization in terms of photocurrent for each of its different regions. To do so, they were scanned with a point light source while the rest of the pixel was kept in darkness. The point source area, A_{ps}, was approximated to a square with side l_{ps} for simplicity. All the photodiodes are reverse-biased and measured through the reset transistors by a Keithley picoammeter voltage source and the rest of the electronics is switched off. Since all the reset transistors share the drain node, the response of all photodiodes is measured in the output at the same time. Consequently, it is expected to read the corresponding photocurrent and a small dark current component. However, this

additional current is minimized by a careful set-up placed in an empty dark room and avoiding undesirable light sources from the equipment.

The experimental set-up, Figure 3.2, consists of an optical part for illumination and observation of the sample (Device Under Test, DUT) and a mechanical part for its precise positioning, requiring the following elements,

- a nonlinear Photonic-Crystal Fiber (PCF) laser
- collimation optics
- a beamsplitter cube
- a microscope lens
- a hexapod platform
- a PCB (Printed Circuit Board)
- a picoammeter/voltage source

The DUT is illuminated by a laser beam of variable power generated by a PCF laser. Up to 8 different wavelength values can be selected simultaneously by an acousto-optic modulator (AOM). The coupling between AOM and optical set-up is realized through three different exchangeable single mode polarization maintaining (SM/PM) fibers (blue, red, and near-infrared). The illumination path leads from the fiber to the radiation sensitive DUT via collimation optics, beamsplitter cube, and microscope lens. The surface of the DUT with the projected light spot is observed through the same microscope lens with observation path through the beamsplitter cube and a tube lens mounted to a digital camera. For the coaxial white light illumination of the chip surface, necessary for taking microphotographic pictures as in Figure 3.3, a second beamsplitter is used (not depicted in Figure 3.2). The DUT is packaged in a JLCC68 (68 pin) to fit the JLCC68 socket in the PCB and the board is attached to the platform of the hexapod, which can be positioned in 6 axes. The microscope lens is mounted to the body of the hexapod. The whole assembly is moved by two linear stages, so the DUT region under the laser illumination can be adjusted. A photograph of the sample under the optical set-up is shown in Figure 3.4.

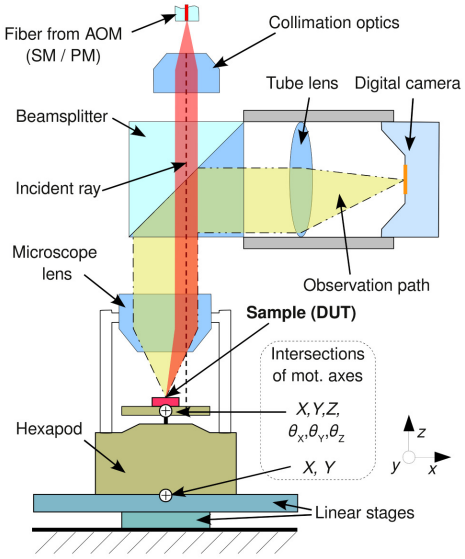


Figure 3.2: Scheme of the optical set-up.

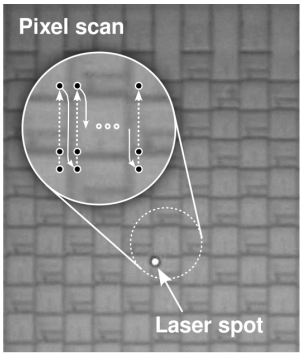


Figure 3.3: Microphotograph of the image sensor matrix with the laser spot and the scanned pixel region within the photodiode.

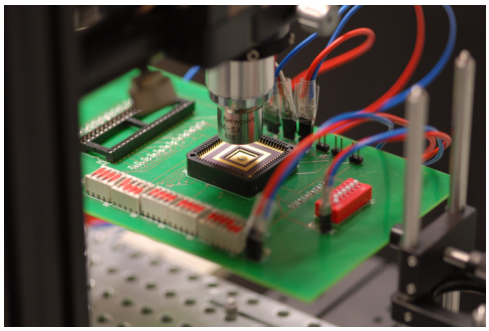


Figure 3.4: Optical set-up and DUT.

3.2 Analytical model

In this section, an analytical expression of the photocurrent of p-n junctions under point source illumination is achieved by solving the steady-state continuity equation in the different regions of the pixel. The main objective is to model the total current through these devices under a light spot impinging perpendicularly onto the top surface in order to gain information regarding the relative importance of these contributions on the overall photocurrent, given by the sum of the different contributions of the single aimed regions. As the light spot is smaller than a pixel, the response depending on the illuminated pixel region can be observed. Moreover, the importance of the peripheral contribution to the total photoresponse can be studied. In this way, if the pixel is scanned with a point source as shown in Figure 3.3, four different regions can be differentiated: the electronics, the active area, the lateral depletion region and the surroundings.

3.2.1 Electronics

As photocarriers are not likely to be generated in the electronics region, the response is assumed to be close to zero when only this region is illuminated. Then, the output current is equal to the saturation current of the inversely biased p-n junctions in the test array, which is given by the following equation for each photodiode

$$I_{\mathrm{o}} = q\left(x_{\mathrm{ph}}^2 + 4x_{\mathrm{ph}}y_{\mathrm{j}}\right)\left(\frac{D_{\mathrm{n}}}{L_{\mathrm{n}}}n_{\mathrm{p0}} + \frac{D_{\mathrm{p}}}{L_{\mathrm{p}}}p_{\mathrm{n0}}\right) \tag{3.1}$$

where D_n and D_p are the electron and hole diffusion coefficients, L_n and L_p are the electron and hole diffusion lengths, and x_{ph}^2 and $4x_{ph}y_j$ are the bottom and side-wall areas of the junction, respectively. This current is negligible and henceforth it will not be considered.

3.2.2 Active area

The calculation of the output current density when the active area is illuminated is based on an ideal solution of the drift–diffusion semiconductor device equations under the following assumptions:

- depletion and abrupt junction approximations are valid
- low-level injection conditions exist in the quasi-neutral regions, meaning that the variation of majority carrier concentration can be neglected there
- the electric field is zero outside the depletion region
- the quasi-neutral regions are uniformly doped
- hole and electron mobilites are constant

Then the steady-state continuity equation in one dimension is solved in the quasi-neutral regions, as the minority carriers mainly move there by diffusion:

$$D_n \frac{\partial^2(n_p - n_{p0})}{\partial y^2} - \frac{n_p - n_{p0}}{\tau_n} + G(y) = 0 \tag{3.2}$$

where n_p and n_{p0} are the electron concentration and its equilibrium value, respectively, τ_n is the electron lifetime, and $G(y)$ is the optical generation rate, Equation (1.2). The generic solution of Equation (3.2) is:

$$n_p(y) = n_{p0} + \frac{\Phi_0 \alpha \tau_n}{1 - \alpha^2 L_n^2} e^{-\alpha y} + A e^{-y/L_n} + B e^{y/L_n} \tag{3.3}$$

and the procedure is analogous for holes in the n region

$$p_n(y) = p_{n0} + \frac{\Phi_0 \alpha \tau_p}{1 - \alpha^2 L_p^2} e^{-\alpha y} + C e^{-y/L_p} + D e^{y/L_p} \tag{3.4}$$

The previous equations must be solved under adequate boundary conditions to derive the particular solution. As suggested in the literature [92],

$$\begin{aligned} p_{\mathrm{n}}(0) &= p_{\mathrm{n0}} + \frac{D_{\mathrm{p}}}{S_{\mathrm{p}}} \left.\frac{\partial p_{\mathrm{n}}}{\partial y}\right|_{y=0} \\ p_{\mathrm{n}}(y_{\mathrm{j}}) &= p_{\mathrm{n0}} e^{qV_{\mathrm{PD}}/KT} \\ n_{\mathrm{p}}(y_{\mathrm{j}}+W) &= n_{\mathrm{p0}} e^{qV_{\mathrm{PD}}/KT} \\ n_{\mathrm{p}}(y_{\mathrm{w}}) &= n_{\mathrm{p0}} - \frac{D_{\mathrm{n}}}{S_{\mathrm{n}}} \left.\frac{\partial n_{\mathrm{p}}}{\partial y}\right|_{y=y_{\mathrm{w}}} \end{aligned} \tag{3.5}$$

where V_{PD}, K, T, S_{n} and S_{p} are the inverse-biased voltage of the photodiode, Boltzmann constant, temperature and the surface recombination velocity of electrons and holes, respectively. However, some simplifications are frequently used. For instance, as recombination is typically higher at a semiconductor surface, the surface recombination velocity is set to infinity for the sake of simplicity,

$$p_{\mathrm{n}}(0) = p_{\mathrm{n0}} \tag{3.6}$$

Also, as recombination is further enhanced by the presence of a metal, a boundary condition fixed by the presence of a metal contact is given at the bottom of the device,

$$n_{\mathrm{p}}(\infty) = n_{\mathrm{p0}} \tag{3.7}$$

Thus, Equation (3.3) and Equation (3.4) are solved subjected to the following boundary conditions for a p-n^{+} junction,

$$\begin{aligned} n_{\mathrm{p}}(\infty) &= n_{\mathrm{p0}} & n_{\mathrm{p}}(y_{\mathrm{j}}+W) &= n_{\mathrm{p0}} e^{qV_{\mathrm{PD}}/KT} \\ p_{\mathrm{n}}(0) &= p_{\mathrm{n0}} & p_{\mathrm{n}}(y_{\mathrm{j}}) &= p_{\mathrm{n0}} e^{qV_{\mathrm{PD}}/KT} \end{aligned} \tag{3.8}$$

However, Equation (3.4) must be rewritten to distinguish between diffusion and well regions for the p-N$_{\mathrm{well}}$ junctions:

$$p_{\mathrm{n}}(y) = \begin{cases} p_{\mathrm{n1}}(y), & 0 \le y \le y_{\mathrm{ph}} \\ p_{\mathrm{n2}}(y), & y_{\mathrm{ph}} \le y \le y_{\mathrm{j}} \end{cases} \tag{3.9}$$

where

$$\begin{aligned} p_{\mathrm{n1}}(y) &= p_{\mathrm{n01}} + \frac{\Phi_0 \alpha \tau_{\mathrm{p}}}{1-\alpha^2 L_{\mathrm{p1}}^2} e^{-\alpha y} + C_1 e^{-y/L_{\mathrm{p1}}} + D_1 e^{y/L_{\mathrm{p1}}} \\ p_{\mathrm{n2}}(y) &= p_{\mathrm{n02}} + \frac{\Phi_0 \alpha \tau_{\mathrm{p}}}{1-\alpha^2 L_{\mathrm{p2}}^2} e^{-\alpha y} + C_2 e^{-y/L_{\mathrm{p2}}} + D_2 e^{y/L_{\mathrm{p2}}} \end{aligned} \tag{3.10}$$

In this way, the following boundary conditions are used to achieve the solution of Equation (3.10) for p-N_{well} junctions:

$$\begin{aligned} J_{\mathrm{p}} &= -qD_{\mathrm{p1}}\left.\frac{\partial p_{\mathrm{n1}}(y)}{\partial y}\right|_{y_{\mathrm{ph}}} = -qD_{\mathrm{p2}}\left.\frac{\partial p_{\mathrm{n2}}(y)}{\partial y}\right|_{y_{\mathrm{ph}}} \\ p_{\mathrm{n1}}(y_{\mathrm{ph}}) &= p_{\mathrm{n2}}(y_{\mathrm{ph}}) \\ p_{\mathrm{n}}(0) &= p_{\mathrm{n01}} \\ p_{\mathrm{n}}(y_{\mathrm{j}}) &= p_{\mathrm{n02}}e^{qV_{\mathrm{PD}}/KT} \end{aligned} \tag{3.11}$$

Finally, the spatial distributions of the quasi-neutral region contributions to the current density are calculated as follows

$$J_{\mathrm{n}}(y) = qD_{\mathrm{n}}\frac{\partial n_{\mathrm{p}}(y)}{\partial y} \qquad J_{\mathrm{p}}(y) = -qD_{\mathrm{p}}\frac{\partial p_{\mathrm{n}}(y)}{\partial y} \tag{3.12}$$

On the other hand, in the depletion region carriers mainly move by drift. The high electric field inside this region moves charges out to neutral regions before they can recombine. Consequently, the photogenerated current density in the depletion region can be found by integrating the generation rate over the region depth, W,

$$J_{\mathrm{w}} = q\int_{y_{\mathrm{j}}}^{y_{\mathrm{j}}+W} G(y)\mathrm{d}y = q\Phi_0 e^{-\alpha y_{\mathrm{j}}}\left(1-e^{-\alpha W}\right) \tag{3.13}$$

The total current must be constant throughout the device, and the different components remain constant along the depletion region. In conclusion, the total current density due to the active area illumination, I_{aa}, can be calculated as sum of drift and diffusion currents in the edges of the depletion region:

$$J = J_{\mathrm{p}}\left(y_{\mathrm{j}}\right) + J_{\mathrm{w}} + J_{\mathrm{n}}\left(y_{\mathrm{j}}+W\right) \tag{3.14}$$

The total current is found by integrating the current density over the point source area, A_{ps}, which was approximated to a square with side l_{ps},

$$I_{\mathrm{aa}} = \int_0^{l_{\mathrm{ps}}}\int_0^{l_{\mathrm{ps}}} J\mathrm{d}x\,\mathrm{d}z = A_{\mathrm{ps}}J \tag{3.15}$$

3.2.3 Lateral depletion region

Regarding the lateral depletion region illumination, the resulting total current I_{W} is calculated by integrating the generation rate over the volume of the depletion region under the aimed

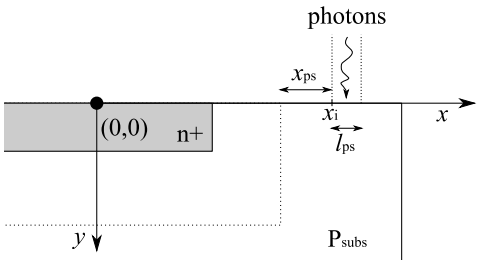


Figure 3.5: Illumination of the surroundings of the photodiode.

area of the surface, A_{ps},

$$I_W = q\int_0^{l_{ps}}\int_0^{l_{ps}}\int_0^{y_j+W} G(y)\mathrm{d}y\,\mathrm{d}x\,\mathrm{d}z = qA_{ps}\Phi_0\left(1-e^{-\alpha(y_j+W)}\right) \tag{3.16}$$

3.2.4 Surroundings

Finally, the point source can aim at the surroundings of the photodiode at a point $x = x_i$ between the edge of the lateral depletion region and the limit of the photodetector region, see Figure 3.5. The boundary condition at this point is the result of solving the steady-state continuity equation, shown in Equation (3.2), under the boundary conditions $n_p(y=0) = n_p(\infty) = n_{p0}$:

$$n_p(x_i,y) = n_{p0} + \frac{\Phi_0\alpha\tau_n}{1-\alpha^2L_n^2}\left(e^{-\alpha y} - e^{-y/L_n}\right) \tag{3.17}$$

Therefore, the minority carriers distribution in the surroundings of the photodiode is achieved solving the steady-state continuity equation in x direction with the previous assumptions and under the following boundary conditions

$$D_n\frac{\partial^2(n_p-n_{p0})}{\partial x^2} - \frac{n_p-n_{p0}}{\tau_n} = 0 \tag{3.18}$$

$$\begin{aligned} n_p\left(\frac{x_{ph}}{2}+W_\ell\right) &= n_{p0}e^{qV_{PD}/KT} \qquad n_p(x_i) = n_p(x_i,y) \qquad (\text{p-n}^+)\\ n_p\left(\frac{x_{well}}{2}+W_\ell\right) &= n_{p0}e^{qV_{PD}/KT} \qquad n_p(x_i) = n_p(x_i,y) \qquad (\text{p-N}_{well}) \end{aligned} \tag{3.19}$$

and the current density due to illumination in x_i is

$$J(x,y) = qD_n\frac{\partial n_p(x,y)}{\partial x} \tag{3.20}$$

Finally, the total lateral current component is found integrating the current density at the boundary of the depletion region, $\frac{x_{\text{ph}}}{2}+W_\ell$ and $\frac{x_{\text{well}}}{2}+W_\ell$ for p-n$^+$ and p-N$_{\text{well}}$, respectively, over the lateral junction area and over the point source side, l_{ps},

$$\begin{aligned} I_{\text{lateral}} &= \int_{l_{\text{ps}}} \left(\int_0^{l_{\text{ps}}} \int_0^{y_{\text{j}}} J\left(\frac{x_{\text{ph}}}{2}+W_\ell, y\right) \mathrm{d}y\,\mathrm{d}z \right) \mathrm{d}x_{\text{i}} \qquad \text{(p-n}^+\text{)} \\ I_{\text{lateral}} &= \int_{l_{\text{ps}}} \left(\int_0^{l_{\text{ps}}} \int_0^{y_{\text{j}}} J\left(\frac{x_{\text{well}}}{2}+W_\ell, y\right) \mathrm{d}y\,\mathrm{d}z \right) \mathrm{d}x_{\text{i}} \qquad \text{(p-N}_{\text{well}}\text{)} \end{aligned} \tag{3.21}$$

where

$$\begin{aligned} J\left(\frac{x_{\text{ph}}}{2}+W_\ell, y\right) &= q\frac{D_{\text{n}}}{L_{\text{n}}}\left[n_{\text{p0}}\left(1-e^{qV_{\text{PD}}/KT}\right) + \frac{\Phi_0 \alpha \tau_{\text{n}}}{1-\alpha^2 L_{\text{n}}^2} \frac{e^{-\alpha y}-e^{-y/L_{\text{n}}}}{\sinh\left(\frac{x_{\text{ps}}}{L_{\text{n}}}\right)} \right] \qquad \text{(p-n}^+\text{)} \\ J\left(\frac{x_{\text{well}}}{2}+W_\ell, y\right) &= q\frac{D_{\text{n}}}{L_{\text{n}}}\left[n_{\text{p0}}\left(1-e^{qV_{\text{PD}}/KT}\right) + \frac{\Phi_0 \alpha \tau_{\text{n}}}{1-\alpha^2 L_{\text{n}}^2} \frac{e^{-\alpha y}-e^{-y/L_{\text{n}}}}{\sinh\left(\frac{x_{\text{ps}}}{L_{\text{n}}}\right)} \right] \qquad \text{(p-N}_{\text{well}}\text{)} \end{aligned} \tag{3.22}$$

and $x_{\text{ps}} = x_{\text{i}} - \frac{x_{\text{ph}}}{2} - W_\ell$ for p-n$^+$ and $x_{\text{ps}} = x_{\text{i}} - \frac{x_{\text{well}}}{2} - W_\ell$ for p-N$_{\text{well}}$, Figure 3.5.

3.3 Results

3.3.1 Experimental validation

Pixels in UMC 90 nm standard technology were fabricated and measured under a point source illumination to validate the accuracy of the proposed model. The measurements were obtained in collaboration with the Fraunhofer Institute for Integrated Circuits IIS in Erlangen and its Design Automation Division EAS in Dresden.

The process dependent parameters of the model were estimated for a 90 nm technology in order to make a comparison with the test chip measurements. Table B.8 and Table B.9 summarize the values used for the model parameters for p-n$^+$ p-N$_{\text{well}}$ junction photodiodes, respectively.

A 8×8 μm^2 area which contains several pixels with $x_{\text{ph}} = 0.76$ μm p-n$^+$ junction photodiodes was exposed to a light source with $\lambda = 500$ nm and $P_{\text{opt}} = 175000$ W/m^2. The region was scanned by moving the hexapod table with the attached DUT in the xy plane (Figure 3.2) in both directions as depicted in Figure 3.3. The point source is about $l_{\text{ps}} = 1.2$ μm width, and

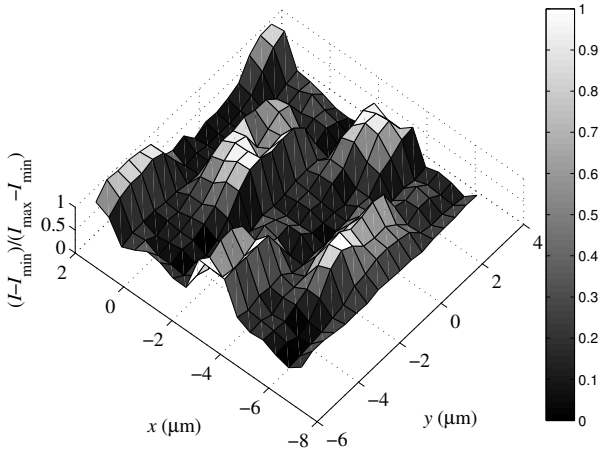


Figure 3.6: Normalized local relative photoresponse as a function of scan coordinates for a region with p-n$^+$ junctions with $x_{ph} = 0.76$ μm and $x_\ell = 4$ μm.

a step size of 0.50 μm defines the scanning resolution. As a result, the relative photocurrent scan of the region of interest of the DUT was obtained, Figure 3.6, where I_{max} is the maximum photoresponse. The origin of coordinates (0,0) in Figure 3.6 corresponds to the centre of a photodiode like in Figure 3.1. The minimum photocurrent due to the electronics illumination, I_{min}, was characterized and subtracted from the measurements to normalize the data for the sake of comparison with the analytical approximation. The light areas of the surface plot represent the highest photoresponse due to the photodiode illumination. As can be seen, the peaks on the plot correspond to the location of the photodiodes present in the scanned area.

Figure 3.7 represents an orthogonal cut of the previous three-dimensional plot together with the analytical estimation given by the proposed model. The minor disagreement in the centre of the photodiode is attributed to the presence of a contact in the fabricated device, so that the light penetration in silicon under this area is expected to be reduced by the presence of metal. This assumption is further reinforced by the fact that the side length of the contact is 0.12 μm, which coincides with this region. Apart from that, both the experimental and theoretical photoresponse showed a maximum response in the border of the p-n$^+$ junction. This result gives an evidence of the importance of the lateral current contribution in small

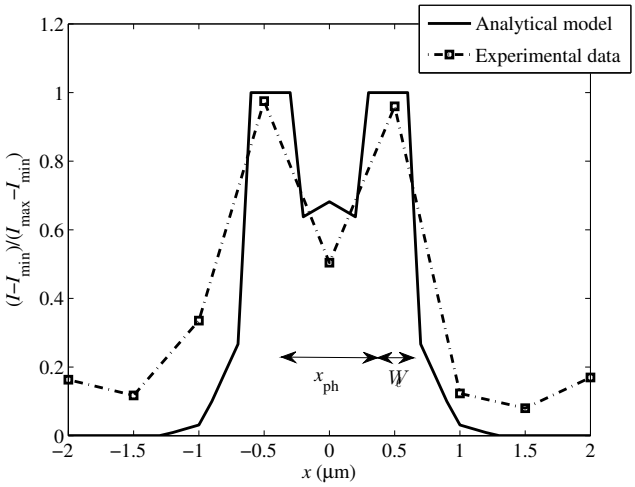


Figure 3.7: Experimental versus theoretical local relative photoresponse as a function of scan coordinates for a p-n$^+$ junction with $x_{ph} = 0.76\mu$m and $x_\ell = 4\mu$m.

photodiodes. The model predicts the same result for different values of λ within the visible range.

A similar procedure was applied to scan a 5×5 μm^2 area which contains pixels with $x_{ph} = 1.28$ μm and $x_{well} = 2.20$ μm p-N$_{well}$ junction photodiodes. It was exposed to the same light source but the laser spot was around $l_{ps} = 0.4$ μm. A step size of 0.33 μm defines the scanning resolution, giving the relative photocurrent depicted in Figure 3.8. Once again, the dark and light areas represent the response of the electronics and the scanned photodiodes, respectively, the origin (0,0) corresponds to the centre of a photodiode, and the minimum photocurrent, I_{min}, was subtracted from the measurements.

An orthogonal cut of the previous figure and the theoretical photoresponse are shown in Figure 3.9. As occurred with the p-n$^+$ photodiodes, the experimental data present the drop in the centre of the photodiode where the contact is placed. However, for p-N$_{well}$ photodiodes the model shows a higher disagreement with regard to the lateral photoresponse modelling. As this device is wider than the previous p-n$^+$ junction and the depletion region is closer to the border of the photodiode region with the electronics, the excess of measured photocurrent is attributed to dark current crosstalk.

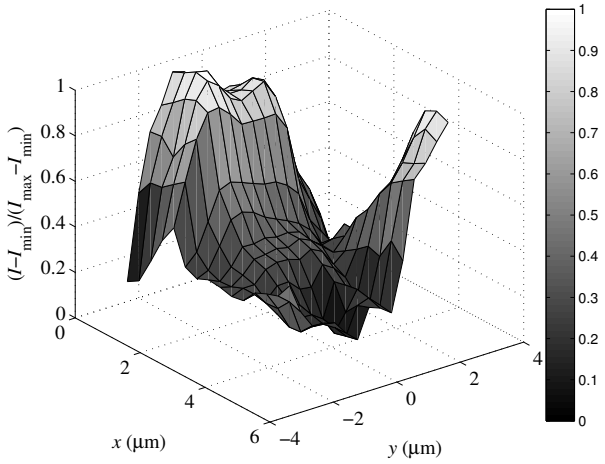


Figure 3.8: Normalized local relative photoresponse as a function of scan coordinates for a region with p-N_{well} junctions with $x_{ph} = 1.28$ μm, $x_{well} = 2.20$ μm and $x_\ell = 4$ μm.

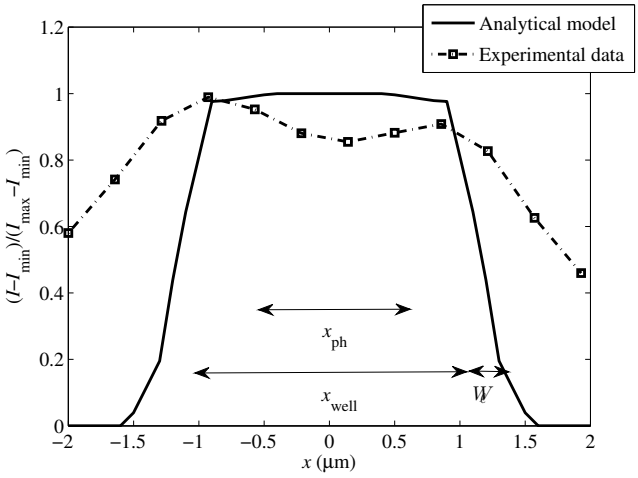


Figure 3.9: Experimental versus theoretical local relative photoresponse as a function of scan coordinates for a p-N_{well} junction with $x_{ph} = 1.28$ μm, $x_{well} = 2.20$ μm and $x_\ell = 4$ μm.

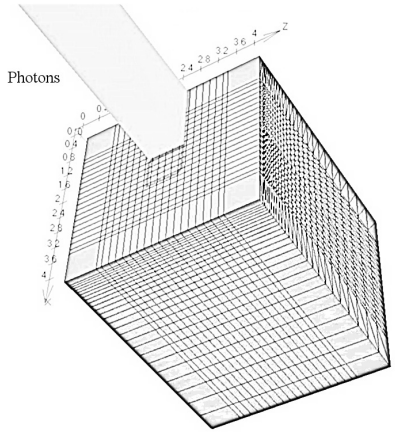


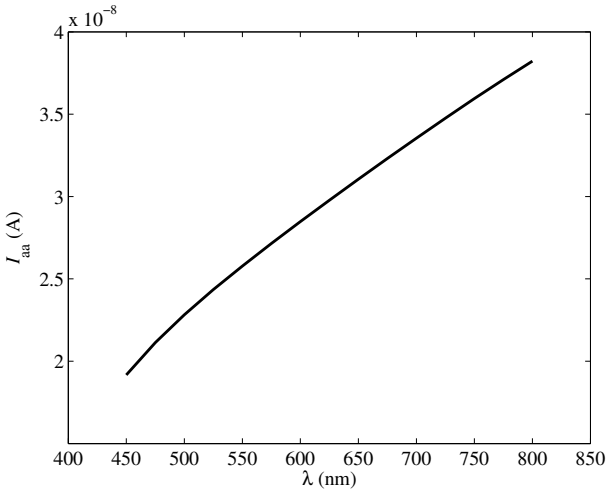
Figure 3.10: Scheme of the simulation set-up. Only the surrounding areas of the junction are illuminated.

3.3.2 Simulation results

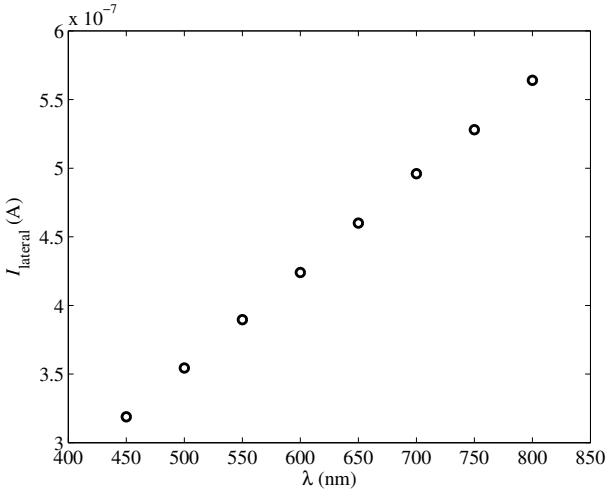
The lateral current collection of small CMOS photodiodes was also studied through three-dimensional simulation results using ATLAS from Silvaco, [93], in collaboration with the Department of Electronics and Computer Technology of the University of Granada. ATLAS is a device simulation framework which is currently widespread used at academic environments and companies. The three-dimensional device simulator of ATLAS, Device3D, integrates the module Luminous3D, which is an advanced simulator used to model absorption and photogeneration in semiconductor devices with arbitrary topology in three dimensions.

In order to isolate the lateral component of the total photocurrent the simulation set-up depicted in Figure 3.10 was used, where only the area surrounding a p-n^+ junction is exposed to the light source, while the n^+ diffusion is not illuminated. A spectral analysis of a cell with $x_{\text{ph}} = 0.76$ μm and $x_\ell = 4$ μm under uniform illumination impinging at the surroundings of the junction was performed. The value of the process dependent and geometrical parameters are those used by the model.

Further evidence of the importance of the lateral component on the overall response was found when analysing the simulation results in Figure 3.11. As observed, the lateral contribution becomes comparable and even higher than the active area response in the visible range. The active area contribution was calculated by the current density integration over the active



(a) Active area photocurrent given by the model.



(b) Lateral photocurrent given by the simulation results.

Figure 3.11: Comparison of the active area and lateral photocurrents given by the model and the simulation results, respectively, for a p-n$^+$ junction with $x_{\text{ph}} = 0.76$ μm and $x_\ell = 4$ μm under uniform illumination conditions.

area, x_{ph}^2, as indicated in Equation (3.15). This suggests that the lateral effects can not longer be neglected for photodiodes in deep sub-micron and nano technologies, highlighting the need for a full two-dimensional analytical model under uniform illumination conditions.

3.4 Conclusions

An analytical sub-pixel study of p-n junctions was performed, solving the one-dimensional steady-state continuity equation in the different regions of the device. The model was compared with experimental data of p-n^+ and p-N_{well} junction photodiodes fabricated in UMC 90 nm standard technology and measured under a point source illumination. Both the model and the measurements revealed a high response due to the illumination of the surroundings of the junction.

Further evidence of the importance of the peripheral collection in small photodiodes was found through three-dimensional device simulation using ATLAS. The p-n^+ photodiode was simulated under uniform illumination of the surroundings of the junction. The results were compared with the photocurrent due to the active area collection, showing a higher response.

Summarizing, both the sub-pixel analysis and the device simulations showed that the peripheral collection should be taken into account for small p-n junction photodiodes. In order to obtain a general model to predict the behaviour of p-n^+ CMOS photodiodes including these phenomena, an analytical study of the lateral collection is developed in Chapter 4.

CHAPTER 4

PHOTODIODE ANALYTICAL MODEL: UNIFORM ILLUMINATION

The previous chapters have put into evidence the importance of the lateral collection on the overall pixel response for small CMOS photodiodes and the necessity of a comprehensive analytical model of these devices which can be easily extended to different photodiode sizes, geometries and technological nodes. The development of a compact, general and scalable model is therefore one of the main goals of this work. It is not straightforward, however, to put this work into context given that there is a large variety of analytical models for photodetectors in the literature which can be classified according to different criteria such us the dimension (1D, 2D or 3D), the kind of device (vertical, lateral, mesa, finger, backside illuminated, etc.), the sort of junction (p-n^+, n-p^+, p-N_{well}, N_{well}-p^+, p-epi-N_{well}, p-epi-P_{well}-n^+, etc.), the application range (gamma ray, X-ray, ultraviolet, visible, infrared, microwave, etc.), and other characteristics. Moreover, boundary conditions and simplifications may vary from one model to another further complicating the classification. This work in particular is focused on vertical CMOS p-n^+ junction photodiodes operated in the visible range and has as distinguishing features the mathematical treatment of lateral collection and the solution of the 2D steady-state equation.

One of the first analytical models for photodiodes based on the solution of the steady-state continuity equation dates from 1977, [42]. Although the study focuses on small photodiodes, for its time, their 50-200 μm wide size will make them bulky for nowadays standards. Besides, the device considered is an InSb p-n^+ mesa structure photodiode and the study is limited to

the substrate. However, this work constitutes to the best of our knowledge the first attempt to study the peripheral photocurrent and its dependence on parameters such as the minority carrier diffusion length and the surface recombination velocity through numerical solution.

More recent studies include fairly elemental 1D models in SPICE. A photodiode model for DC as well as high frequency circuit simulation was presented in [94]. The photocurrent is given by a very simple expression in terms of the quantum efficiency. The accuracy of the model was verified with the measured data obtained from p-n^+ and p-N_{well} photodiodes fabricated using a conventional 0.25 μm CMOS technology. The devices considered, however, have a diameter of 75 μm, large enough to conceal peripheral effects. Another analytical model for PSPICE simulation was developed in [95]. Both p-n^+ and p-N_{well} structures were studied by solving the steady-state response. The model was verified for a large 1cm^2 area device by comparing the PSPICE circuit simulations to results from the Medici numerical semiconductor device simulator. More useful models are found in [92] and [96]. In both papers the steady-state continuity equation is solved in the different regions of the device under similar boundary conditions. In the former, p-epi-N_{well} and p-epi-P_{well}-n^+ photodiodes were fabricated using the TSMC 0.5 μm CMOS technology. The effect of the surface recombination velocity is studied to avoid an inadequate value affected by the surface defects in the manufacture process. The latter presents the definition and implementation of a n-p^+ photodiode SPICE model and was validated by comparison with numerical device simulations using DESSIS of ISE-TCAD. Simulation results were also compared with experimental data from a p-n^+ photodiode including a SiO_2-Si_3N_4 antireflecting coating optimized for near-infrared applications and a PIN photodiode for X-ray imaging applications.

All the previous models neither include an analytical solution of the peripheral photocurrent nor mention it, except for [42]. Taking this phenomenon into account requires at least a two-dimensional treatment of the problem which constitutes a challenge from a mathematical point of view. Although this will be the approach followed in this work, a brief description of previous studies on the peripheral collection with varying approaches over mesa, lateral, finger, and backside illuminated photodiodes apart from vertical ones is included for the sake of completeness.

An array of p-n lateral finger photodiodes was studied in [44]. The symmetry of the structure, in addition to other assumptions, simplifies the calculation of the lateral collection. In particular, the term in the diffusion equation representing the variation of the diffusion current flowing in the vertical direction of the film is neglected and constant optical genera-

tion rate within the thin film is assumed. Consequently, the diffusion equation is effectively reduced to one dimension. Some years later, the same author presented a theory for the enhanced photoresponse of p-n junctions that arises from the lateral diffusion of photogenerated carriers [97]. The p-n junction is in a periodical mesa structure, which imposes particular boundary conditions. The solution is a complex set of relations which are more useful by considering some special cases. These particular solutions are compared with the results of numerical analysis. It was found that the magnitude of the peripheral photoresponse is sensitive to geometric and physical factors such as semiconductor thickness, surface recombination, optical absorption length, and competition for photogenerated carriers by adjacent photodiodes. Moreover, an increase of the lateral collection significance for smaller devices is predicted. Lateral photodiodes were also the subject of study in [98], where an electrical model was proposed. The resolution of the continuity equation in this case was divided into two parts: an electrical solution, which corresponds to the one-dimensional solution without generation term, and a photonic solution, which represents the two-dimensional solution with the generation term. The results are compared to an approximated one-dimensional classical approach confirming that a two-dimensional model is needed. The transport and continuity equation for generated carriers within a two-dimensional structure was also solved in [99] to develop an analytical model for finger p-NBL(N-Buried-Layer)-P_{well}-n^+ photodiodes. Simplifying assumptions were introduced for each of the device regions as, for instance, the no y-dependence in the N-Buried-Layer and P-substrate. The continuity equation was solved in the region n^+ applying the technique of separation of variables and the same procedure is supposedly used for the P_{well} between two n^+ diffusions, although the solution is not reported. Numerical device simulations from ATLAS show good agreement with the carrier concentration given by the model, which was also successfully compared with measurements of the structure under consideration fabricated in a 0.6 μm BiCMOS process.

Although the previous two-dimensional models are of interest because they deal with the peripheral phenomenon in different ways, they are specific for lateral, mesa and finger structures. Next, three different works dealing with vertical photodiodes are revised. In [43], a quantitative description of the photocurrent of a p-n^+ photodiode was developed based on [44] particularized for the case of a thin film substrate. The analysis makes use of the fact that the current density at the peripheral edges of the photodiode in a closely spaced array has a maximum value near the surface and decays approximately in a linear fashion with the depth into the substrate. Simulation data of the current density using Davinci^{TM} are used to prove this as-

sumption. Finally, the photocurrent given by experimental measurements in a 0.5 μm CMOS technology is compared with the derived expression, demonstrating that the correspondence improves due to the lateral collection. Beyond the previous quantitative approach, an analytical charge collection model was derived in [45] to assess the impact of the photodiode size, doping profile and surface recombination velocity on the Modulation Transfer Function (MTF) and the charge collection efficiency of a p-n^+ junction. The transmittance is considered as unity and the photogeneration function includes a sinusoidal term to facilitate MTF extraction. Additional symmetry conditions are imposed in order to use Green's functions to solve the two-dimensional steady-state continuity equation. Although the calculated MTF results agree well with measured data of fabricated imagers based on three different pixel designs in a 0.5 μm CMOS process, the final expression is only barely outlined and cannot be easily used. MTF modelling was also considered in [46]. In this case, the model is based on a two-dimensional diffusion equation solution and covers the impact of the pixel active area geometrical shape. However, the two-dimensional analysis is limited to the substrate under the diffusion area. The solution of the one-dimensional problem is taken as a boundary condition in the centre of the device, while the symmetrical photocarriers diffusion effect within the substrate is considered as a second boundary condition. The theoretical prediction is compared with results obtained by means of a sub-micron scanning system from P_{well}-n^+ photodiode APSs fabricated in a standard CMOS 0.35 μm technology.

Finally, there are very few works which tackle the problem of the three-dimensional continuity equation resolution. In [47], a vertical n-p^+ photodiode is described by a three-dimensional analytical model based on Fourier analysis under the constraints of periodic illumination and mesa structure array. The work focuses on the substrate and the symmetry implies particular boundary conditions. The accuracy of the predictions was proved using measured data for HgCdTe and InSb photodiodes. Based on this work, a three-dimensional model was presented in [100], as the second part of a work in which a one-dimensional analysis of p^+-epi-n^+ photodiodes was derived, [101]. The analytical solution was verified with numerical simulations using Medici and based on parameters extracted from a standard 0.35 μm CMOS process. In the second part of the paper, investigation of lateral photoresponse using linear photodiode arrays and numerical device simulations was presented, illustrating the importance of surface recombination and mobility degradation along the Si-SiO_2 interface.

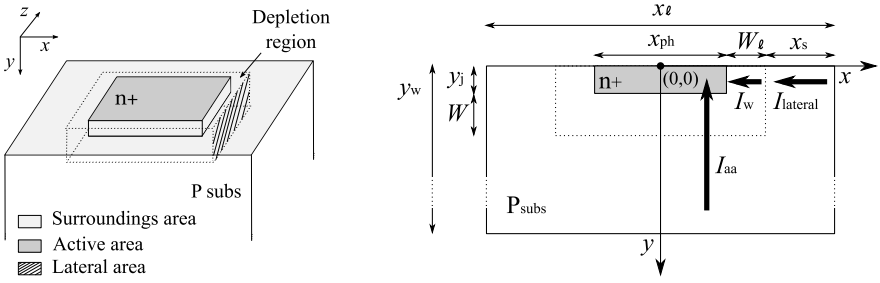
In this chapter, a fully analytical two-dimensional model that describes the lateral collection through the side-walls of the junction of a single CMOS photodiode operating in the

visible range is developed. It accounts for surface recombination effects through the definition of appropriate boundary conditions. The model assumes uniform illumination conditions of a single photodiode and therefore, considerations of lateral crosstalk do not apply in this case. As a result, a compact analytical solution is found which is suitable for integration in Computer Aided Design (CAD) environments, as we will demonstrate in Chapter 5. Besides, the model is validated using both ATLAS simulation and experimental results from fabricated photodiodes in AMS 180 nm and UMC 65 nm CMOS standard technologies.

4.1 Test structures and experimental set-up

This study is based on the photoresponse of p-n$^+$ junction photodiodes with different sizes operating under uniform illumination in the visible range. Moreover, the photodiodes are characterized by their small dimensions, with junction depth y_j and thickness y_w, such as the one in Figure 4.1. The n$^+$ diffusion and the whole device are x_{ph} and x_ℓ wide, respectively. In reverse-bias operation three main regions are distinguished: two quasi-neutral regions and the depletion region with thickness W (in y-direction) and W_ℓ (in x-direction). The depletion region is assumed to be located in the substrate because of its lower doping concentration.

Squared p-n$^+$ junctions in AMS 180 nm and UMC 65 nm standard technologies were fabricated and measured. The set of fabricated photodiodes in each technology is summarized in Table 4.1. The smallest photodiode allowed by the technology design rules is included in



(a) 3D photodiode scheme which includes the different regions of the device.

(b) Cross-section of the photodiode where the dimensions and the different current components are indicated.

Figure 4.1: Photodiode structure.

x_{ph} (μm)	x_s (μm)
0.56	0.35
	0.60
	0.85
	1.10
	1.35
1.06	0.35
	0.60
	0.85
	1.10
	1.35
1.56	0.85
2.06	0.35
	0.60
	0.85
	1.10
	1.35
2.56	0.35
	0.60
	1.10
	1.35

x_{ph} (μm)	x_s (μm)
0.56	0.355
	0.605
	0.855
	1.105
	1.355
	1.605
1.06	0.355
	0.605
	0.855
	1.105
	1.355
	1.605
1.56	0.355
	0.605
	0.855
	1.105
	1.355
2.06	0.355
	0.605
	0.855
	1.105
	1.355
2.56	0.355
	0.605
	0.855
	1.105
	1.355
3.06	0.355
	0.605

Table 4.1: Parameters of the fabricated p-n$^+$ junction photodiodes in AMS 180 nm (left) and UMC 65 nm (right) standard technologies.

both cases. More details of the test structures, CHIP 3 and CHIP 4, are given in Section 1.4.2.

The measurements were carried out using a experimental set-up which consists of the following elements:

– a Diode Pumped Solid State (DPSS) laser

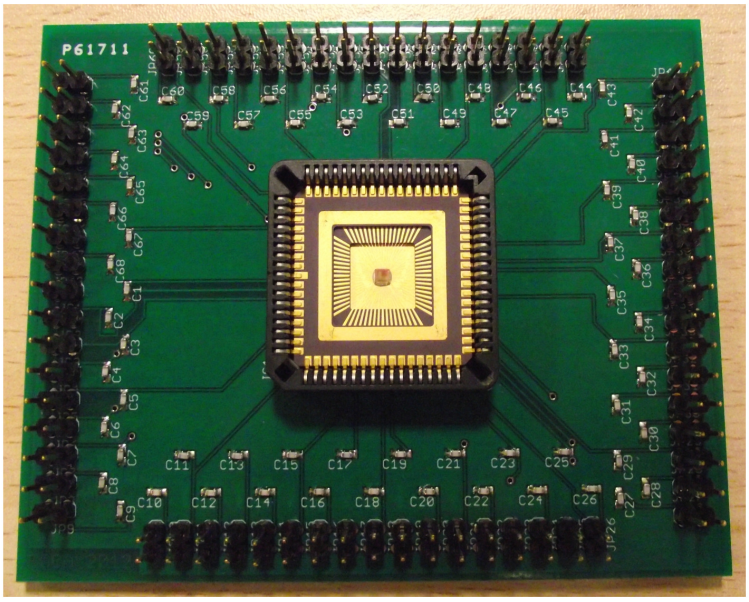


Figure 4.2: Printed circuit board designed to measure the CHIP 3 and CHIP 4.

- a mirror
- a platform
- a PCB (Printed Circuit Board)
- a picoammeter/voltage source

A 532 nm DPSS laser which produces a laser beam with a 400 W/m^2 power density was used. A mirror oriented at 45^o to the incoming laser beam redirects light through the DUT (Device Under Test) surface. The DUT consists of a chip, which is packaged in a JLCC68 (68 pin) to fit the JLCC68 socket in the PCB, Figure 4.2. In order to expose the photodiodes to the laser beam, the board is fixed to a two-axis platform with two 10 µm resolution heads. Finally, the devices are polarized one by one and their current is read by a Keithley 6487 picoammeter voltage source.

4.2 Analytical model of the lateral photocurrent

4.2.1 Problem formulation

In order to study the static characteristic of the devices such as the ones introduced in the previous section, the steady-state equations that describe their transport features were solved. The total steady-state current of the photodiode in the reverse operation regime comprises the following components: the active area current (I_{aa}), the lateral depletion region current (I_W), and the lateral current ($I_{lateral}$).

The photocurrent due to the active area exposure is given by the diffusion of minority carriers and generation of electron-hole pairs in the depletion region, and it can be calculated as follows,

$$I_{aa} = q x_{ph}^2 \left(\int_{y_j}^{y_j+W} G(y)\mathrm{d}y + D_n \left.\frac{\partial n_p}{\partial y}\right|_{y_j+W} - D_p \left.\frac{\partial p_n}{\partial y}\right|_{y_j} \right) \tag{4.1}$$

where n_p and p_n are the electron and hole concentration, D_n and D_p are the electron and hole diffusion coefficients and $G(y)$ is the optical generation rate, Equation (1.2). The minority carrier concentrations are calculated by the one-dimensional steady-state continuity equation resolution in the quasi-neutral regions, as explained in Chapter 3. There is another contribution related to the active area size, which is the peripheral collection through the bottom of the depletion region due to the photocarriers generated deep in the substrate. This last term is not considered in this study, but it is expected to be significant for photodiodes with a larger junction area and illumination sources with a larger wavelength.

Regarding the lateral depletion region, the high electric field in this volume moves charges out to neutral regions before they can recombine. The current generated in this region where carriers mainly move by drift can be found by integrating the generation rate over the whole region for the n_{sides} of the junction, Figure 4.1(b),

$$I_W = n_{sides}\, q \int_{-\frac{x_{ph}}{2}}^{\frac{x_{ph}}{2}} \int_0^{W_\ell} \int_0^{y_j+W} G(y)\mathrm{d}y\mathrm{d}x\mathrm{d}z \tag{4.2}$$

However, this term proved out to be not very significant, as it will be shown in Section 4.3.

Finally, the lateral current, $I_{lateral}$, is caused by the photocarriers generated in the surroundings of the photodiode that reach the junction by diffusion. This phenomenon is most pronounced in small photodiodes due to the increase of the side-walls-to-active area ratio. As it will be demonstrated, its magnitude is comparable to the active area current, I_{aa}, for small

photodiodes, showing a strong dependence with the dimension of the active area in relation to the collecting surrounding area.

4.2.2 Mathematical solution to lateral collection

The aim of this analysis is to develop a model for the lateral photocurrent, I_{lateral}, through the device under uniform illumination impinging perpendicularly onto the top surface. To do so, a square-shaped photodiode was considered without loss of generality, $n_{\text{sides}} = 4$. The surroundings of the photodiode form four lateral p-n junctions in the x and z directions, Figure 4.1(a). Consequently, the steady state two-dimensional continuity equation has to be solved,

$$\frac{\partial^2(n_{\text{p}} - n_{\text{p0}})}{\partial x^2} + \frac{\partial^2(n_{\text{p}} - n_{\text{p0}})}{\partial y^2} - \frac{n_{\text{p}} - n_{\text{p0}}}{\tau_{\text{n}} D_{\text{n}}} + \frac{G(y)}{D_{\text{n}}} = 0 \tag{4.3}$$

where n_{p0} is the equilibrium electron concentration and τ_{n} is the electron lifetime. For convenience, Equation (4.3) is rewritten as,

$$\frac{\partial^2 N}{\partial x^2} + \frac{\partial^2 N}{\partial y^2} - \frac{N}{L_{\text{n}}^2} = -\kappa f(y) \tag{4.4}$$

where $L_{\text{n}} = \sqrt{\tau_{\text{n}} D_{\text{n}}}$ is the minority carrier diffusion length, $N = n_{\text{p}} - n_{\text{p0}}$ is the minority carrier excess concentration, $\kappa = \frac{\alpha \Phi_0}{D_{\text{n}}}$ and $f(y) = e^{-\alpha y}$.

To solve Equation (4.4) the following boundary conditions at the borders of the surrounding area are applied,

$$N\left(\frac{x_{\text{ph}}}{2} + W_\ell, y\right) = -n_{\text{p0}} \qquad N\left(\frac{x_\ell}{2}, y\right) = 0 \tag{4.5}$$

At the bottom of the device a boundary condition fixed by the presence of a metal contact is given,

$$N(x, y_{\text{w}}) = 0. \tag{4.6}$$

The boundary condition at the surface is usually expressed as, $N(x,0) = \frac{D_{\text{n}}}{S_{\text{n}}} \left.\frac{\partial N}{\partial y}\right|_{y=0}$ where S_{n} is the surface recombination velocity. However, the introduction of this term leads to unmanageable expressions when a multidimensional analysis is attempted making it necessary to resort to numerical methods [42, 100]. In order to obtain a fully analytical solution the following boundary condition is used,

$$N(x,0) = \gamma \frac{D_{\text{n}}}{S_{\text{n}}} \tag{4.7}$$

where γ is a fitting parameter. The suitability of this assumption will be conveniently justified in Section 4.3.

The solution of Equation (4.4) under boundary conditions (4.5)-(4.7) constitutes a nonhomogeneous problem, which is solved applying the method of separation of variables, [102],

$$N(x,y) = u(x,y) + v(y) \tag{4.8}$$

Inserting Equation (4.8) in Equation (4.4), the following expression is obtained,

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 v}{\partial y^2} - \frac{u}{L_{\mathrm{n}}^2} - \frac{v}{L_{\mathrm{n}}^2} = -\kappa f(y) \tag{4.9}$$

In a similar way, the substitution of N in the boundary conditions (4.5)-(4.7) yields

$$\begin{aligned} u\left(\frac{x_{\mathrm{ph}}}{2} + W_\ell, y\right) + v(y) &= -n_{\mathrm{p0}} \\ u\left(\frac{x_\ell}{2}, y\right) + v(y) &= 0 \\ u(x, y_{\mathrm{w}}) + v(y_{\mathrm{w}}) &= 0 \\ u(x,0) + v(0) &= \gamma \frac{D_{\mathrm{n}}}{S_{\mathrm{n}}} \end{aligned} \tag{4.10}$$

Thus, if $v(y)$ is the solution of the problem

$$\left.\begin{aligned} \frac{\partial^2 v}{\partial y^2} - \frac{v}{L_{\mathrm{n}}^2} &= -\kappa f(y) \\ v(y_{\mathrm{w}}) &= 0 \\ v(0) &= \gamma \frac{D_{\mathrm{n}}}{S_{\mathrm{n}}} \end{aligned}\right\} \tag{4.11}$$

then $u(x,y)$ must satisfy

$$\left.\begin{aligned} \frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} - \frac{u}{L_{\mathrm{n}}^2} &= 0 \\ u(x, y_{\mathrm{w}}) &= 0 \\ u(x,0) &= 0 \\ u\left(\frac{x_{\mathrm{ph}}}{2} + W_\ell, y\right) &= -n_{\mathrm{p0}} - v(y) \\ u\left(\frac{x_\ell}{2}, y\right) &= -v(y) \end{aligned}\right\} \tag{4.12}$$

Equation (4.11) is a second-order nonhomogeneous linear ordinary differential equation and its solution is achieved applying the method of variation of constants:

$$\begin{aligned} v(y) = & \frac{-\gamma\frac{D_\mathrm{n}}{S_\mathrm{n}}e^{-\frac{y_\mathrm{w}}{L_\mathrm{n}}} + \frac{\kappa}{\frac{1}{L_\mathrm{n}^2}-\alpha^2}\left(e^{-\frac{y_\mathrm{w}}{L_\mathrm{n}}} - e^{-\alpha y_\mathrm{w}}\right)}{e^{\frac{y_\mathrm{w}}{L_\mathrm{n}}} - e^{-\frac{y_\mathrm{w}}{L_\mathrm{n}}}} e^{\frac{y}{L_\mathrm{n}}} \\ & + \frac{\gamma\frac{D_\mathrm{n}}{S_\mathrm{n}}e^{\frac{y_\mathrm{w}}{L_\mathrm{n}}} + \frac{\kappa}{\frac{1}{L_\mathrm{n}^2}-\alpha^2}\left(e^{-\alpha y_\mathrm{w}} - e^{\frac{y_\mathrm{w}}{L_\mathrm{n}}}\right)}{e^{\frac{y_\mathrm{w}}{L_\mathrm{n}}} - e^{-\frac{y_\mathrm{w}}{L_\mathrm{n}}}} e^{-\frac{y}{L_\mathrm{n}}} \\ & + \frac{\kappa}{\frac{1}{L_\mathrm{n}^2}-\alpha^2} e^{-\alpha y} \end{aligned} \tag{4.13}$$

On the other hand, Equation (4.12) is a second-order homogeneous partial differential equation in two independent variables. In order to find a solution, it is assumed a separable solution in the form

$$u(x,y) = X(x)Y(y) \tag{4.14}$$

Substituting Equation (4.14) into Equation (4.12) it is obtained

$$\frac{\mathrm{d}^2X}{\mathrm{d}x^2}Y + X\frac{\mathrm{d}^2Y}{\mathrm{d}^2y} - \frac{XY}{L_\mathrm{n}^2} = 0 \tag{4.15}$$

and dividing the previous equation by XY

$$\frac{1}{X}\frac{\mathrm{d}^2X}{\mathrm{d}x^2} = \frac{1}{L_\mathrm{n}^2} - \frac{1}{Y}\frac{\mathrm{d}^2Y}{\mathrm{d}y^2} \tag{4.16}$$

The left-hand side of Equation (4.16) depends only upon x, and the right side is a function of y only. So, differentiating Equation (4.16) with respect to x or y,

$$\frac{\mathrm{d}}{\mathrm{d}x}\left(\frac{1}{X}\frac{\mathrm{d}^2X}{\mathrm{d}x^2}\right) = 0 \tag{4.17}$$

Integration of the previous equation yields

$$\frac{1}{X}\frac{\mathrm{d}^2X}{\mathrm{d}x^2} = \sigma \tag{4.18}$$

where σ is a separation constant. From Equation (4.16) and Equation (4.18),

$$\frac{1}{L_\mathrm{n}^2} - \frac{1}{Y}\frac{\mathrm{d}^2Y}{\mathrm{d}y^2} = \sigma \tag{4.19}$$

Equation (4.18) and Equation (4.19) can be rewritten as,

$$\frac{\mathrm{d}^2X}{\mathrm{d}x^2} - \sigma X = 0 \tag{4.20}$$

and

$$\frac{\mathrm{d}^2Y}{\mathrm{d}y^2} - \left(\frac{1}{L_\mathrm{n}^2} - \sigma\right) Y = 0 \tag{4.21}$$

Thus, $u(x,y)$ is the solution of Equation (4.12) if $X(x)$ and $Y(y)$ are the solutions of the ordinary differential equations Equation (4.20) and Equation (4.21), respectively. In a similar way, the boundary conditions are separated as follows,

$$\begin{aligned} X(x)Y(0) = 0 &\Rightarrow Y(0) = 0 \\ X(x)Y(y_\mathrm{w}) = 0 &\Rightarrow Y(y_\mathrm{w}) = 0 \\ X\left(\frac{x_\ell}{2}\right) Y(y) &= -v(y) \\ X\left(\frac{x_\mathrm{ph}}{2} + W_\ell\right) Y(y) &= -n_\mathrm{p0} - v(y) \end{aligned} \tag{4.22}$$

To determine $X(x)$ and $Y(y)$ an eigenvalue problem must be solved. The values of σ and $\left(\frac{1}{L_\mathrm{n}^2} - \sigma\right)$ which produce nontrivial solutions must be found. These are the possible cases,

i) $\frac{1}{L_\mathrm{n}^2} - \sigma > 0 \Rightarrow \sigma > 0$, $\sigma = 0$ or $\sigma < 0$

ii) $\frac{1}{L_\mathrm{n}^2} - \sigma = 0 \Rightarrow \sigma > 0$

iii) $\frac{1}{L_\mathrm{n}^2} - \sigma < 0 \Rightarrow \sigma > 0$

If $\frac{1}{L_\mathrm{n}^2} - \sigma > 0$, case i), the general solution of Equation (4.21) is of the form

$$Y(y) = Ae^{\sqrt{\frac{1}{L_\mathrm{n}^2} - \sigma}\, y} + Be^{-\sqrt{\frac{1}{L_\mathrm{n}^2} - \sigma}\, y} \tag{4.23}$$

where A and B are arbitrary constants. To satisfy the boundary conditions the following system of equations holds,

$$\begin{aligned} A + B &= 0 \\ Ae^{\sqrt{\frac{1}{L_\mathrm{n}^2} - \sigma}\, y_\mathrm{w}} + Be^{-\sqrt{\frac{1}{L_\mathrm{n}^2} - \sigma}\, y_\mathrm{w}} &= 0 \end{aligned} \tag{4.24}$$

The determinant of this system is different from zero. Consequently, A and B must both be zero, and hence, the general solution $Y(y)$ is identically zero. The solution is trivial and therefore not of interest.

If $\frac{1}{L_{\mathrm{n}}^2} - \sigma = 0$, case ii), the general solution is

$$Y(y) = A + By \tag{4.25}$$

Making use of the boundary conditions,

$$\begin{aligned} A &= 0 \\ A + By_{\mathrm{w}} &= 0 \end{aligned} \tag{4.26}$$

the solution is thus zero again.

Finally, if $\frac{1}{L_{\mathrm{n}}^2} - \sigma < 0$, case iii), the general solution is

$$Y(y) = A\cos\left(\sqrt{\sigma - \frac{1}{L_{\mathrm{n}}^2}}y\right) + B\sin\left(\sqrt{\sigma - \frac{1}{L_{\mathrm{n}}^2}}y\right) \tag{4.27}$$

From the condition $Y(0) = 0$, $A = 0$. The condition $Y(y_{\mathrm{w}}) = 0$ gives

$$B\sin\left(\sqrt{\sigma - \frac{1}{L_{\mathrm{n}}^2}}y_{\mathrm{w}}\right) = 0 \tag{4.28}$$

For nontrivial solutions, that is $B \neq 0$, the following condition holds,

$$\sqrt{\sigma - \frac{1}{L_{\mathrm{n}}^2}}y_{\mathrm{w}} = n\pi, \qquad n = 1,2,3,... \tag{4.29}$$

or

$$\sigma_n = \frac{1}{L_{\mathrm{n}}^2} + \theta_n^2, \qquad n = 1,2,3,... \tag{4.30}$$

where $\theta_n = \frac{n\pi}{y_{\mathrm{w}}}$. For this infinite set of discrete values of σ, the problem has a nontrivial solution. Therefore, the solutions of Equation (4.21) are,

$$Y_n(y) = B_n\sin(\theta_n y) \tag{4.31}$$

On the other hand, the general solution of Equation (4.20) for $\sigma = \sigma_n > 0$ may be written as given below,

$$X_n(x) = C_n e^{\sqrt{\sigma_n}x} + D_n e^{-\sqrt{\sigma_n}x} \tag{4.32}$$

where C_n and D_n are arbitrary constants. Thus, the functions

$$u_n(x,y) = X_n(x)Y_n(y) \tag{4.33}$$

satisfy Equation (4.12). They can be rearranged using $a_n = B_n C_n$ and $b_n = B_n D_n$ as

$$u_n(x,y) = \left(a_n e^{\sqrt{\sigma_n}x} + b_n e^{-\sqrt{\sigma_n}x}\right)\sin(\theta_n y) \tag{4.34}$$

and, since Equation (4.12) is linear and homogeneous, the infinite series

$$u(x,y) = \sum_{n=1}^{\infty}\left(a_n e^{\sqrt{\sigma_n}x} + b_n e^{-\sqrt{\sigma_n}x}\right)\sin(\theta_n y) \tag{4.35}$$

is also a solution by means of the superposition principle. Constants a_n and b_n are determined from the remaining boundary conditions,

$$u\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell, y\right) = \sum_{n=1}^{\infty}\left[\left(a_n e^{\sqrt{\sigma_n}\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell\right)} + b_n e^{-\sqrt{\sigma_n}\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell\right)}\right)\sin(\theta_n y)\right] = -n_{\mathrm{p0}} - v(y) \tag{4.36}$$

$$u\left(\frac{x_\ell}{2}, y\right) = \sum_{n=1}^{\infty}\left[\left(a_n e^{\sqrt{\sigma_n}\frac{x_\ell}{2}} + b_n e^{-\sqrt{\sigma_n}\frac{x_\ell}{2}}\right)\sin(\theta_n y)\right] = -n_{\mathrm{p0}} - v(y) \tag{4.37}$$

and they will be satisfied if $v(y)$ can be represented by Fourier sine series. The coefficients are calculated by solving the following system of equations,

$$\begin{aligned} a_n e^{\sqrt{\sigma_n}\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell\right)} + b_n e^{-\sqrt{\sigma_n}\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell\right)} &= \frac{1}{y_{\mathrm{w}}}\int_{-y_{\mathrm{w}}}^{y_{\mathrm{w}}}(-n_{\mathrm{p0}} - v(y))\sin(\theta_n y)\mathrm{d}y \\ a_n e^{\sqrt{\sigma_n}\frac{x_\ell}{2}} + b_n e^{-\sqrt{\sigma_n}\frac{x_\ell}{2}} &= \frac{1}{y_{\mathrm{w}}}\int_{-y_{\mathrm{w}}}^{y_{\mathrm{w}}}(-n_{\mathrm{p0}} - v(y))\sin(\theta_n y)\mathrm{d}y \end{aligned} \tag{4.38}$$

The resulting expressions for the a_n and b_n coefficients are,

$$\begin{aligned} a_n &= V\frac{e^{-\sqrt{\sigma_n}\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell\right)} - e^{-\sqrt{\sigma_n}\frac{x_\ell}{2}}}{2\sinh\left(\sqrt{\sigma_n}x_{\mathrm{s}}\right)} \\ b_n &= V\frac{e^{\sqrt{\sigma_n}\frac{x_\ell}{2}} - e^{\sqrt{\sigma_n}\left(\frac{x_{\mathrm{ph}}}{2}+W_\ell\right)}}{2\sinh\left(\sqrt{\sigma_n}x_{\mathrm{s}}\right)} \end{aligned} \tag{4.39}$$

where

$$V = (-1)^n\frac{2\theta_n}{y_{\mathrm{w}}}\left[-\frac{\gamma\frac{D_{\mathrm{n}}}{S_{\mathrm{n}}}\cosh\left(\frac{y_{\mathrm{w}}}{L_{\mathrm{n}}}\right)}{\sigma_n} + \frac{\kappa}{\frac{1}{L_{\mathrm{n}}^2}-\alpha^2}\left(\frac{\cosh\left(\frac{y_{\mathrm{w}}}{L_{\mathrm{n}}}\right)-e^{-\alpha y_{\mathrm{w}}}}{\sigma_n} - \frac{\sinh(\alpha y_{\mathrm{w}})}{\alpha^2+\theta_n^2}\right)\right] \tag{4.40}$$

and $x_{\mathrm{s}} = \frac{x_\ell}{2} - \frac{x_{\mathrm{ph}}}{2} - W_\ell$ represents the distance between the edge of the depletion region and the limit of the photodiode, that is, the region surrounding the junction in which collected carriers contribute to the lateral current, see Figure 4.1(b).

Once $u(x,y)$ and $v(y)$, and hence $N(x,y)$, have been calculated, an analytical expression for the current density is obtained as

$$J_{\mathrm{n}}(x,y) = qD_{\mathrm{n}}\frac{\partial N(x,y)}{\partial x} \tag{4.41}$$

resulting in,

$$J_{\mathrm{n}}(x,y) = qD_{\mathrm{n}}\sum_{n=1}^{\infty}\sqrt{\sigma_n}\left(a_n e^{\sqrt{\sigma_n}x} - b_n e^{-\sqrt{\sigma_n}x}\right)\sin(\theta_n y) \tag{4.42}$$

Finally, the total lateral current component is found integrating the current density at the boundary of the depletion region, $\frac{x_{\mathrm{ph}}}{2} + W_\ell$, over the n_{sides} side-walls

$$I_{\mathrm{lateral}} = n_{\mathrm{sides}}\int_{-\frac{x_{\mathrm{ph}}}{2}}^{\frac{x_{\mathrm{ph}}}{2}}\int_0^{y_{\mathrm{j}}} J_{\mathrm{n}}\left(\frac{x_{\mathrm{ph}}}{2} + W_\ell, y\right)\mathrm{d}y\mathrm{d}z \tag{4.43}$$

For a squared device, $n_{\mathrm{sides}} = 4$, Equation (4.43) yields

$$I_{\mathrm{lateral}} = \frac{8x_{\mathrm{ph}}qD_{\mathrm{n}}}{y_{\mathrm{w}}}\sum_{n=1}^{\infty} I_1\left(y_{\mathrm{w}}\right) I_2\left(x_{\mathrm{s}}\right) I_3\left(y_{\mathrm{j}}\right) \tag{4.44}$$

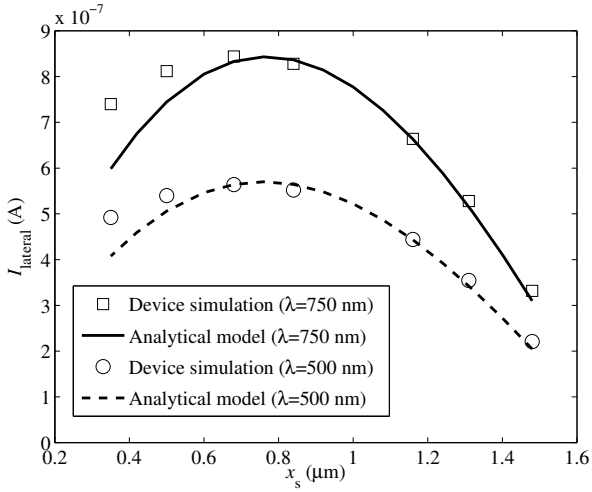
where

$$\begin{aligned} I_1\left(y_{\mathrm{w}}\right) &= (-1)^n\left[-\frac{\gamma\frac{D_{\mathrm{n}}}{S_{\mathrm{n}}}\cosh\left(\frac{y_{\mathrm{w}}}{L_{\mathrm{n}}}\right)}{\sigma_n} + \right. \\ &\left. + \frac{\kappa}{\frac{1}{L_{\mathrm{n}}^2} - \alpha^2}\left(\frac{\cosh\left(\frac{y_{\mathrm{w}}}{L_{\mathrm{n}}}\right) - e^{-\alpha y_{\mathrm{w}}}}{\sigma_n} - \frac{\sinh(\alpha y_{\mathrm{w}})}{\alpha^2 + \theta_n^2}\right)\right] \\ I_2\left(x_{\mathrm{s}}\right) &= \frac{\sqrt{\sigma_n}\left(1 - \cosh\left(\sqrt{\sigma_n}x_{\mathrm{s}}\right)\right)}{\sinh\left(\sqrt{\sigma_n}x_{\mathrm{s}}\right)} \\ I_3\left(y_{\mathrm{j}}\right) &= 1 - \cos(\theta_n y_{\mathrm{j}}) \end{aligned} \tag{4.45}$$

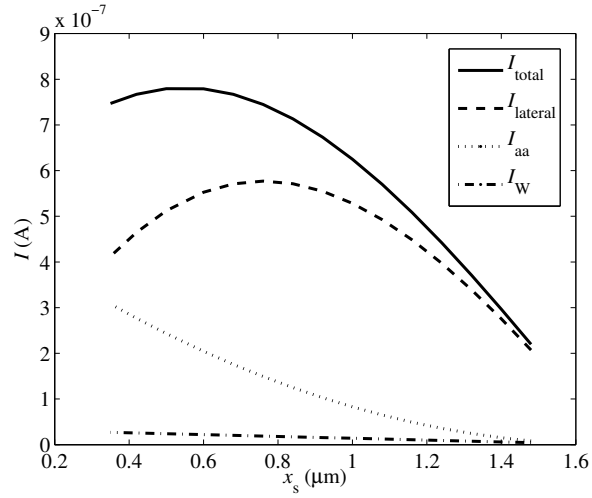
4.3 Model validation

4.3.1 Simulation results

In order to validate the proposed model, three-dimensional numerical device simulations using ATLAS from Silvaco were performed, as described in Section 3.3.2. The technological parameters are estimated for the 90 nm technological node and the values of all parameters of



(a) Comparison of simulation and model results for 500 nm and 750 nm wavelengths in terms of the lateral response as a function of x_s. The symbols correspond to the simulations performed with ATLAS and the lines represent the analytical model description.



(b) Photocurrent components as a function of x_s for $\lambda = 500$ nm.

Figure 4.3: (a) Model validation by comparison with simulations from ATLAS and (b) current components for $\lambda = 500$ nm.

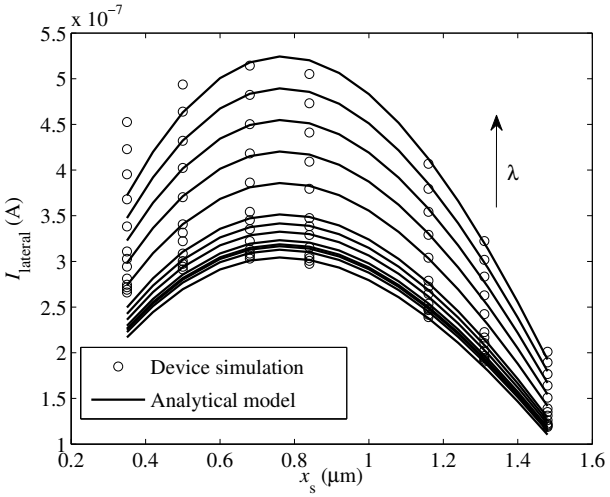


Figure 4.4: Simulation and model results for I_{lateral} versus the surrounding area for $\lambda = [470, 800]$ nm.

the model are given in Table B.10. Simulations under monochromatic illumination with different values of the wavelength and the power of the light source were carried out. A unique squared cell of size $x_\ell = 4$ μm was considered, and different values of x_{ph} were used, resulting in a varying x_{s}.

Regarding the calculation of the lateral current given by the proposed model in Equation (4.44), some remarks are needed. Firstly, $n = 1, 2$ was used in the summation, as the contribution of the remaining terms proved not to be significant. Secondly, the surface recombination velocity is a physical parameter which depends on the illumination wavelength and is not easily estimated, specially for $\lambda < 500$ nm. Making use of the simulation results, the surface recombination velocity was rewritten as a function of the wavelength,

$$S_{\text{n}}(\lambda) = C_1 e^{C_2 \lambda} + C_3 e^{C_4 \lambda} \tag{4.46}$$

Finally, the fitting parameter, γ, of the boundary condition in Equation (4.7) was extracted by comparison with simulation data resulting in a function of both the wavelength and the power of the light source,

$$\gamma(\lambda, P_{\text{opt}}) = C_5 \lambda P_{\text{opt}} \tag{4.47}$$

In doing so, it was observed that $\left.\frac{\partial N}{\partial y}\right|_{y=0}$ values given by the model were close to the ones obtained for γ, consequently confirming the physical consistency of the model and the validity of the assumption for the boundary condition described by Equation (4.7).

Figure 4.3(a) shows the comparison between simulation and model results using a light source with wavelengths of 500 nm and 750 nm. Although the simulation results are in reality the sum of both I_{lateral} and I_{W}, it will be proved that the latter can be neglected. In this figure, the lateral current, I_{lateral}, is plotted against the distance between the edge of the depletion region and the limit of the photodiode, x_{s}, representing the surrounding area. As x_{ℓ} is kept constant, different x_{s} correspond to different values of x_{ph}, which permits the analysis of their joint effect. As can be seen in the figure, the analytical model proposed in this work shows an excellent agreement with the simulation results obtained with ATLAS for both wavelengths, particularly, both simulations and model reflect the strong dependence of the lateral current on the collecting area surrounding the device. This is attributed to the collection of photocarriers diffused from the substrate or generated outside the active area. Nevertheless, the most striking feature is related to the maximum that can be observed for $x_{\text{s}} \approx 0.75\mu\text{m}$. This fact suggests that from the designer's viewpoint there is a trade-off between the photodiode active area and the surrounding collecting area that must be taken into account in order to obtain the maximum photoresponse for small photodiodes. Particularly for those with high-resolution constraints where optimizing the photodiode area to maximize the collection efficiency may result in a significant reduction of the total layout area of the device.

In Figure 4.3(b), the total current, as well as its different components as given by the proposed model, are shown. Inspection of this figure reveals that the main component of the total photocurrent of the device is the lateral contribution. Moreover, the existence of an optimum x_{ph} vs. x_{s} value which maximizes the collection efficiency is also manifested in the total current. On the other hand, as expected, the contribution of the active area itself, I_{aa}, decreases as x_{s} increases due to a reduction in x_{ph}. Finally, the effect of the lateral depletion component, I_{W}, was found to be neglectable, as anticipated in Section 4.1.

It can also be seen that the proposed analytical model lightly underestimates the lateral current for the photodiodes with a smaller surrounding area, corresponding with the left side of the curve, and that this effect increases with larger wavelengths. This minor disagreement is expected to be connected with the peripheral collection through the bottom of the depletion region, which is not modelled. The reason is that collection through the bottom of the depletion region is more significant for larger photodiodes, which present a larger junction area

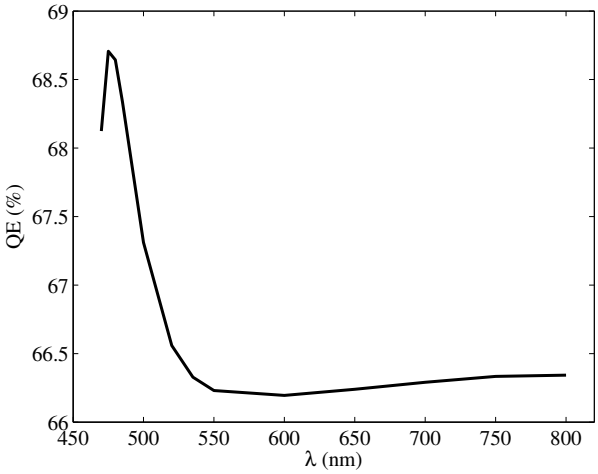


Figure 4.5: Total quantum efficiency.

as well. Besides, light sources with larger wavelengths present a higher penetration depth, which favours bottom collection. The model results in Figure 4.3(a) are in accordance with these facts.

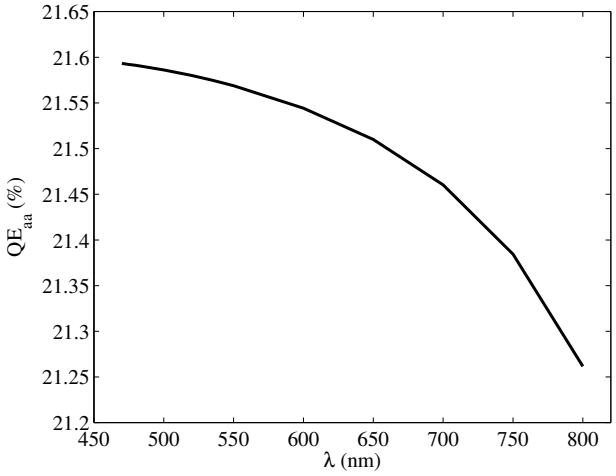
The previous analysis was extended to cover the visible range. To do so, the same structures were simulated under the same conditions varying the wavelength of the light source. The simulation results are plotted with circles in Figure 4.4 against x_s along with the photoresponse given by the proposed model. It was found that all the curves present a maximum response, which corresponds to the same x_s, and its value increases with λ.

The photodiode spectral response is often described in terms of its quantum efficiency, which is defined as the ratio of absorbed photocarriers to the number of injected photons for a specific wavelength, Section 1.2.3,

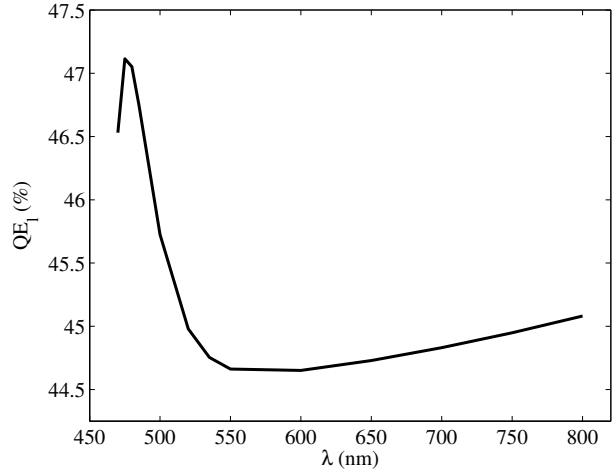
$$\mathrm{QE} = \frac{hcI_{\mathrm{total}}}{\lambda q P_{\mathrm{opt}} A} \tag{4.48}$$

where $A = x_\ell^2$ is the so-called optical window area. The total quantum efficiency can be expressed as the sum of two terms, the quantum efficiency due to the junction under the active area, $\mathrm{QE}_{\mathrm{aa}}$, and quantum efficiency related to the lateral collection, QE_ℓ,

$$\mathrm{QE} = \mathrm{QE}_{\mathrm{aa}} + \mathrm{QE}_\ell = \frac{hcI_{\mathrm{aa}}}{\lambda q P_{\mathrm{opt}} x_\ell^2} + \frac{hc(I_{\mathrm{lateral}} + I_{\mathrm{W}})}{\lambda q P_{\mathrm{opt}} x_\ell^2} \tag{4.49}$$



(a) Quantum efficiency of the active area junction.



(b) Quantum efficiency of the lateral junctions.

Figure 4.6: Quantum efficiency.

Figure 4.5 and Figure 4.6 show the total quantum efficiency and both QE_{aa} and QE_{ℓ}, respectively, for a photodiode with $x_{ph} = 2.4$ μm and $P_{opt} = 10^5$ W/m^2. The results reveal that QE_{ℓ} is the dominant component and QE_{aa} decreases with the illumination wavelength.

4.3.2 Experimental validation

The p-n$^+$ photodiodes described in Section 4.1 were measured under a 400 W/m^2 532 nm uniform illumination given by a DPSS laser thanks to the support of the Centro Singular de Investigación en Tecnoloxías da Información (CITIUS) and the Optics Area of the Department of Applied Physics of the University of Santiago de Compostela. A total of 19 and 11 chips were considered in AMS 180 nm and UMC 65 nm standard technologies, respectively. In order to fully characterize the effect of the lateral component on the overall photocurrent, two types of photosensing structures were fabricated. The first set corresponds to the photodiodes in Table 4.1 while the second set consists of the same photodiodes with metal layers acting as an optical shield over the diffusion to ensure that no charges are collected through the active area, see Section 1.4.2. The response for each photodiode was calculated as the arithmetic mean of these measurements and given in Table 4.2 and Table 4.3 for the structures in AMS 180 nm standard technology and in Table 4.4 and Table 4.5 for the structures in UMC 65 nm standard technology. The measurements obtained show consistent results throughout the devices inspected. There are only four photodiodes in AMS 180 nm technology in which the value of the measured lateral photocurrent is higher than the total current. This fact is attributed to experimental errors during the manipulation of the DUTs.

The green, orange and red colors in the tables are used to highlight the worst, medium and best values of the photoresponse, respectively, as a function of the photodiode diffusion width, x_{ph}, and the distance between the edge of the depletion region and the limit of the photodiode, x_s. If each table is seen as a matrix, the element (1,1) corresponds to the smallest p-n$^+$ junction that can be fabricated for that particular technology fulfilling the technology design rules. From this element, the values of x_{ph} and x_s increase with a step size of 0.50 μm and 0.25 μm, respectively. In other words, the elements (1,2) and (2,1) represent the photoresponse of two different photodiodes with the same value of x_{ℓ}. The same occurs for the elements (1,3), (2,2) and (3,1) and so forth. Hence the data can be visualized as a wavefront expanding from the upper left position where each new front represents an increased value of x_{ℓ}. This fact makes it possible to study the joint effect of x_{ph} and x_s variation over a photodiode with the same total width, x_{ℓ}, as was done in the device simulations presented in Section 4.3.1.

x_{ph} (µm)	x_s (µm)				
	0.35	0.60	0.85	1.10	1.35
0.56	189	234	261	256	208
1.06	264	330	355	367	304
1.56	-	-	300	-	-
2.06	390	474	518	529	495
2.56	318	386	-	450	446

Table 4.2: Total photocurrent (nA) in AMS180 nm standard technology.

x_{ph} (µm)	x_s (µm)				
	0.35	0.60	0.85	1.10	1.35
0.56	135	196	210	220	186
1.06	221	286	311	313	302
1.56	-	-	401	-	-
2.06	333	426	470	476	453
2.56	388	503	-	557	430

Table 4.3: Lateral photocurrent (nA) in AMS180 nm standard technology.

x_{ph} (µm)	x_s (µm)					
	0.355	0.605	0.855	1.105	1.355	1.605
0.56	68	95	102	100	89	52
1.06	172	235	244	247	228	137
1.56	304	419	435	437	405	-
2.06	468	635	663	664	605	-
2.56	505	662	664	683	635	-
3.06	769	736	-	-	-	-

Table 4.4: Total photocurrent (nA) in UMC 65 nm standard technology.

x_{ph} (µm)	x_s (µm)					
	0.355	0.605	0.855	1.105	1.355	1.605
0.56	64	88	89	87	81	48
1.06	156	221	224	220	179	115
1.56	275	387	390	391	354	-
2.06	413	570	578	560	515	-
2.56	411	555	534	537	465	-
3.06	595	577	-	-	-	-

Table 4.5: Lateral photocurrent (nA) in UMC 65 nm standard technology.

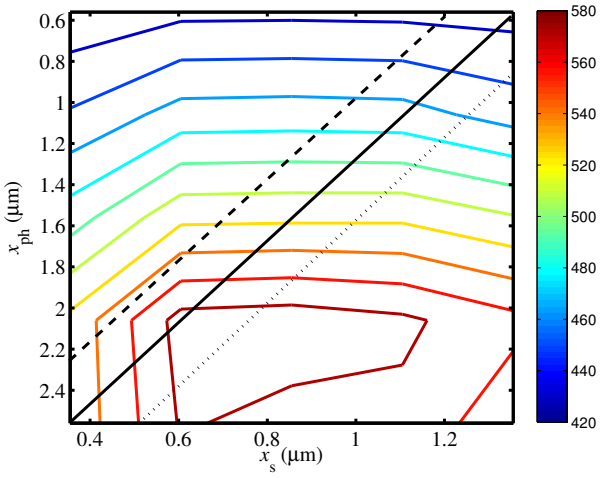
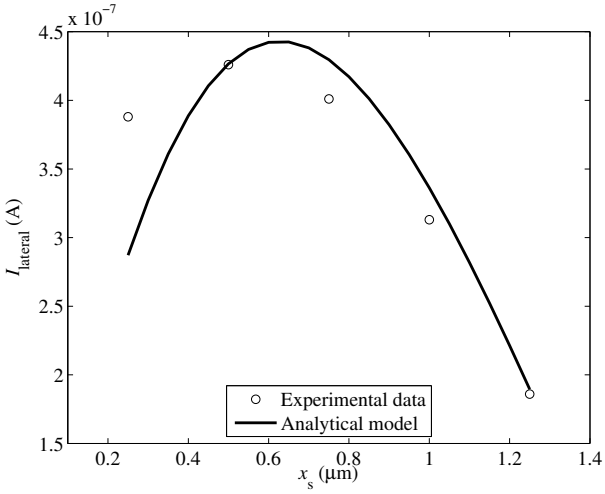


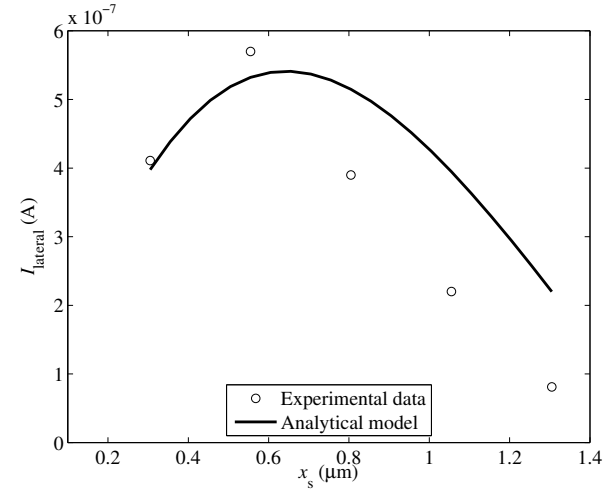
Figure 4.7: Contour map of the lateral photocurrent (nA) in UMC 65 nm standard technology (Table 4.5).

Inspection of the experimental results confirms that the lateral current, Table 4.3 and Table 4.5, dominates the total current, Table 4.2 and Table 4.4, in both technologies, as predicted by the model and device simulations in the previous section. This means that most of the collected photocarriers are generated outside the collecting active area. What is not easy to draw off is the photoresponse dependence on both x_{ph} and x_s parameters. Figure 4.7 represents a contour map of Table 4.5 to illustrate this matter. Each black line drawn over the map goes through the photoresponse of the p-n$^+$ junctions with a particular value of the photodiode total width, x_ℓ. In this way, the devices related to the dashed line are smaller than those represented by the dotted line. This map shows that the maximum value of the contour line crossed by the solid line represents a better solution than the ones corresponding to the dashed line, showing all of them a lower photoresponse, and is as good as the best solutions on the dotted line in terms of photoresponse with the additional advantage of a smaller device. In other words, there is a trade-off between the photodiode diffusion width, x_{ph}, and the distance between the edge of the depletion region and the limit of the photodiode, x_s, which results in an optimum photoresponse with the minimum layout area.

After this quantitative analysis, the proposed model given by Equation (4.44) was compared with these experimental results. The lateral photocurrent for the photodiodes with $x_\ell = 3.26$ µm and $x_\ell = 3.27$ µm in AMS 180 nm and UMC 65 nm standard technologies



(a) AMS 180 nm standard technology.



(b) UMC 65 nm standard technology.

Figure 4.8: Model validation by comparison with experimental results of the lateral response as a function of x_s ($\lambda = 532$ nm).

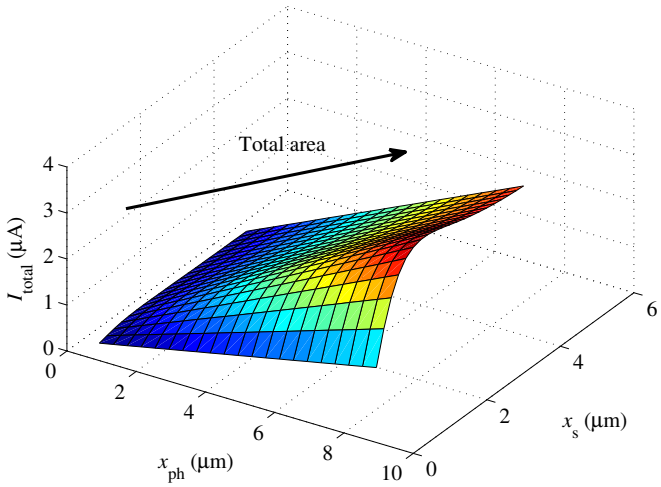


Figure 4.9: Surface plot of the total photocurrent given by the proposed model for the p-n$^+$ junctions in UMC 65 nm standard technology.

is represented with circles in Figure 4.8 against the distance between the edge of the depletion region and the limit of the photodiode, x_s. As predicted by the device simulations in Section 4.3.2, there is an optimum phoresponse in terms of the photodiode diffusion width, x_{ph}, and x_s. Moreover, the proposed analytical model fits the experimental results with an excellent agreement for both technologies, predicting with high accuracy the optimum photodiode geometry to achieve the maximum photoresponse.

To conclude, the total photoresponse for the fabricated p-n$^+$ junctions was verified by the proposed model. Moreover, the response of larger photodiodes beyond the fabricated structures can be predicted using the proposed model. Taking advantage of this functionality, the total modelled photocurrent is plotted in Figure 4.9 as a two dimensional function of x_{ph} and x_s. Consequently, the optimum value of the diffusion which maximizes the photoresponse can be estimated depending on the photodetector total area in a particular design. In this sense, the model proposed in this work constitutes a powerful tool to aid in the design of CMOS imagers. This potential will be further enhanced by the implementation of the model in a hardware description language to be used in computer aided design tools during the design process. This will be the subject of the work in Chapter 5.

4.4 Conclusions

A study of the lateral collection in p-n$^+$ junctions was developed. An analytical model was achieved by solving the two-dimensional steady-state continuity equation in the surroundings of the junction. Device simulations were used to obtain an expression for a fitting parameter in terms of the wavelength and the power of the light source. In addition, the proposed model was validated with experimental results in AMS 180 nm and UMC 65 nm standard technologies.

As a result, it was found that for small photodiodes the photocurrent due to the lateral collection dominates over the other components and this fact is reflected in the total photocurrent. The total quantum efficiency was also calculated, showing a spectral response dominated by the lateral component as well. Furthermore, the lateral photocurrent shows a dependence with the collecting area surrounding the junction and presents a maximum. Consequently, there is a trade-off between the active area and the surroundings for small p-n$^+$ junctions which must be taken into account.

Finally, the implementation of the model in a Hardware Description Language (HDL) is need to be used by designers in Computer Aided Design (CAD) tools. For this reason, the model is implemented in Verilog-AMS and validated by circuit simulations in Chapter 5.

CHAPTER 5

HDL IMPLEMENTATION AND CIRCUIT SIMULATION

In Chapter 4, an analytical model for the photoresponse estimation of p-n^+ junction photodiodes has been developed and validated through experimental results. Since the impact of the layout style on the performance of CMOS circuits and devices is a well-known fact, such effort only acquires significance if the model can be used by designers in Computer Aided Design (CAD) tools. Despite the reverse-biased p-n junction photodiode being one of the most popular types of photodetectors used in CMOS image sensors imagers, there is a lack of a thorough theoretical study addressing fundamental design issues. For this reason, accurate scalable optoelectronic models for photodetectors are essential to verify the correct behaviour of the whole image device by means of circuit simulation in standard CAD tools.

The power and flexibility of current standard Hardware Description Languages (HDLs) offer an effective and efficient way to describe multiple domain and mixed-signal electronic systems and predict their behaviour prior to manufacture. At the moment, the dominant HDLs in the electronics industry are VHDL and Verilog. Although they were developed to be used in the digital domain, nowadays both provide analog and mixed-signal extensions which offer effective means to describe and simulate multi-discipline systems [103]. The extension of the VHDL standard that supports the description and simulation of analog, digital, and mixed-signal circuits and systems is informally known as VHDL-AMS, while Verilog-A and Verilog-AMS are the analog and mixed-signal Verilog extensions, respectively. Compared to SPICE language for circuit simulation, HDLs offer some benefits as the incorporation of

non-electrical mechanisms as far as they can be described with mathematical expressions. Furthermore, the models can be directly interfaced with any circuit simulator owing an appropriate compiler.

Despite the large variety of models for photodectors revised in Chapter 4, there are only a few authors who have presented some attempts to address both the development of photodiode models and their implementation into HDLs. A collection of models for optoelectronic devices, such as lasers and optical fiber, including a model for a high speed InGaAs PIN photodiode and a Buried Double p-n Junction (BDJ) photodiode in VHDL-AMS was presented in [49]. Although the photodiode models are based on commercial devices and the mathematical expressions are not given, the work is a good example of the HDLs potential. A Verilog-A photodiode model was suggested in [50] within the framework of the development of an open source circuit simulator supporting Verilog-A standardization. However, the photocurrent model is not proposed in terms of physical and technological parameters and it must undergo an important characterization process prior to be used as a design element. Finally, several photodetectors and pixel sensors are modelled with VHDL-AMS in [51] and [104], respectively, but the mathematical models follow classical expressions. All the previous models share the characteristic of being based in classical 1D representations of photodetectors and neither of them include 2D lateral effects. In this sense, the HDL implementation of the model proposed in Chapter 4 describing lateral photocurrent effects on small photodiodes with relation to their size and geometry will significantly aid the design process.

Another example of the utility of the Verilog-AMS implementation in the design process of an integrated circuit is given for an analytical model for Enclosed Layout Transistors (ELTs) which was presented in a previous work [53]. Experimental results have shown that the inherent radiation hardness of deep sub-micron processes can be further exploited using transistors with a gate-enclosed layout, [105, 106]. These ELTs have the additional advantage of improving the hot-carrier reliability of CMOS circuits by reducing the drain/source electric field compared to conventionally designed transistors [107]. Although the regions defining the transistor source, gate and drain could, in principle, have any shape, practical considerations encourage the use of regular polygonal shapes of a given number of sides, n, and this was, therefore, the scope of the analysis.

The first attempt to achieve an ELT electrical model was proposed in [108], where different approaches based on variations of the SPICE and BSIM models for standard transistors were developed for long-channel ELT at low drain bias. Later, an approximate numerical solution

in the velocity saturation region of an annular MOSFET was proposed based on a discretized one-dimensional representation of the voltage along the channel [107]. The theoretical predictions of the numerical model were compared with experimental data from square-shape ELT fabricated in a CMOS 0.25 μm process. In [53] and [54] the first fully analytical model for short-channel polygonal ELT was presented, focusing on transistors with small and moderate W/L ratios. Short-channel effects were also considered in the analysis, particularly the threshold voltage reduction due to drain-induced barrier lowering and short-channel effects. The proposed model offers a compact representation of the current of these devices which permits its HDL description to be integrated in CAD tools.

In this chapter, the analytical models for p-n$^+$ junction photodiodes and ELTs are implemented into Verilog-AMS. Their performance is validated by circuit simulation in Cadence framework.

5.1 Verilog-AMS implementation

5.1.1 p-n$^+$ junction photodiode

In order to study the dynamic response of the photodiode, an electrical equivalent circuit of the device is essential. The physical analysis suggests that the photodiode consists of a photocurrent source, I_{ph}, an intrinsic diode and a photodiode capacitance, C_{PD}, Figure 5.1. The photocurrent model was developed in Chapter 4, Equation (4.44), and more details about the photodiode capacitance can be found in Section 1.2.4.

The electrical model was implemented in Verilog-AMS and compiled in Cadence framework for circuit simulation purposes. The Verilog-AMS code is given in Appendix C. Two different Active Pixel Sensors (APSs), whose schematics are depicted in Figure 5.2, were

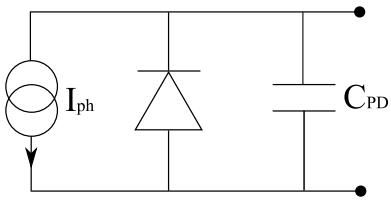
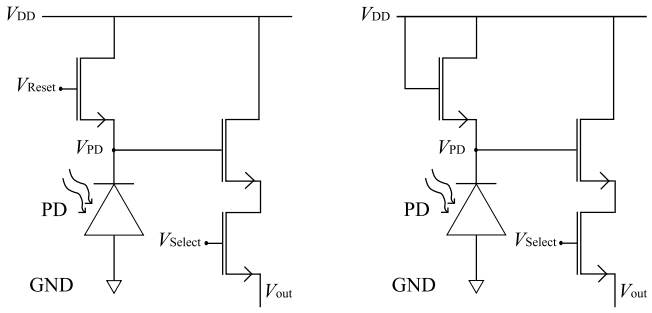


Figure 5.1: Electrical equivalent circuit of the photodiode.



(a) 3T-APS (b) Logarithmic APS

Figure 5.2: 3T-APS and logarithmic APS schemes.

studied using the Cadence Virtuoso AMS-Designer Simulator. The photodiode 3T-APS, Figure 5.2(a), is widely used and it consists of a photodiode and three transistors: the reset transistor, which acts as a switch to reset the photodiode, a source follower, and a select transistor, which allows to address the pixel or a single row of pixels in a matrix configuration. In the integration mode of operation the photodiode capacitance is charged by the reset transistor. When it is switched off, the rate of decay of charge and bias voltage on the photodiode, V_{PD}, depends on the photocurrent due to the incident optical power, I_{ph}, as [63]

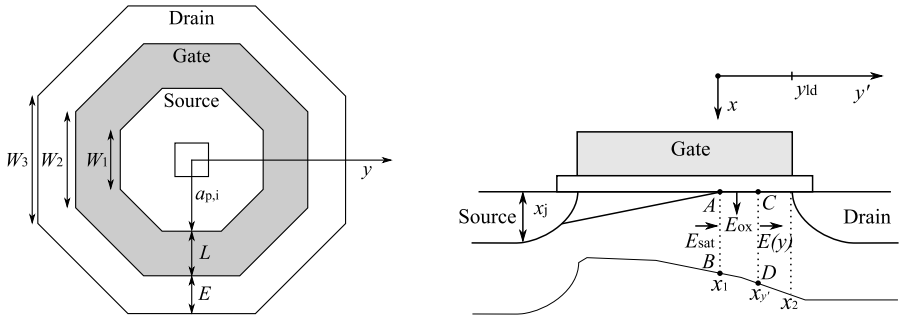
$$\frac{\mathrm{d}V_{\mathrm{PD}}}{\mathrm{d}t} = \frac{I_{\mathrm{ph}}}{C_{\mathrm{PD}}} \tag{5.1}$$

The logarithmic APS configuration is very similar, Figure 5.2(b), but the reset transistor is no longer used in a reset mode because its gate is connected to the drain voltage. Consequently, the naturally linear photogenerated current is converted into a logarithmic voltage by means of the I-V characteristic of the reset transistor operating in subthreshold,

$$V_{\mathrm{PD}} = V_{\mathrm{DD}} - \frac{KT}{q}\ln\left(\frac{I_{\mathrm{ph}}}{I_{\mathrm{s}}}\right) \tag{5.2}$$

where I_{s} is the inverse-bias saturation current. A non-linear output permits a larger dynamic range but a smaller output voltage swing, leading to a low signal-to-noise ratio.

More details of these pixel circuits are given in Section 1.3.2.



(a) Schematic of an ELT device with $n = 8$.

(b) ELT cross-section in saturation.

Figure 5.3: Enclosed-layout transistor scheme.

5.1.2 Gate-Enclosed Layout Transistors (ELTs)

The source and drain diffusions of a standard layout transistor are undistinguishable from each other from a design point of view. On the other hand, Enclosed-Layout Transistors (ELTs) are characterized by having an inner diffusion (either drain or source) surrounded by the transistor channel (gate) and outer diffusion. An example of such a device is shown in Figure 5.3(a), depicting an octagonal ELT ($n = 8$), where the inner diffusion has been taken as the source terminal. Parameters W_1, W_2 and W_3 represent the sides of the regular polygonal shapes defining the source, gate and drain, respectively. $a_{\mathrm{p,i}}$ is the apothem of the inner diffusion, L is the transistor channel length and E is the extension of the outer diffusion over the gate. From the inspection of Figure 5.3(a), it is clear that although the channel length of the device, L, is well defined, there is no direct physical equivalent to the channel width, W, of a standard transistor. However, it is possible to define a generalized expression for the effective W/L ratio of a n-side ELT [53].

The analytical model, developed in a previous work [53], makes use of the two-section approach that divides the channel into two regions: the linear region, from the source terminal to the saturation point, and the saturation region, from the saturation point to the drain terminal.

The saturation region length, y_{ld}, is often referred to as the channel length modulation parameter and determines the magnitude of the drain current in saturation. In this region, the carrier velocities are assumed to increase linearly with the electric field at low levels and to saturate at velocity v_{sat} when the electric field exceeds E_{sat}. The situation is summarized

in Figure 5.3(b), where for the sake of clarity, the origin of coordinates is redefined to be taken at the saturation point A, as $y' = y - (a_{\mathrm{p,i}}/2) - L + y_{\mathrm{ld}}$. C is an arbitrary point along the channel surface between the saturation point and the drain terminal, and B and D represent the non-uniform depletion region widths x_1 and $x_{y'}$ at points A and C, respectively. The depletion width at the drain end is x_2 and $y' = y_{\mathrm{ld}}$, which corresponds to the modulation length.

Under the strong inversion assumption, space-charge I–V model for short channel transistors operating in the linear region was found to be

$$I_{\mathrm{D}} = \left[\frac{W}{L}\right]_{\mathrm{eff}} \mu C_{\mathrm{ox}} \left[\left((V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2}\right) - \frac{4V_{\mathrm{W}}\phi_{\mathrm{F}}}{3}\left(\left(1 + \frac{V_{\mathrm{DS}}}{2\phi_{\mathrm{F}}}\right)^{3/2} - \left(1 + \frac{3V_{\mathrm{DS}}}{4\phi_{\mathrm{F}}}\right)\right)\right] \tag{5.3}$$

where $0 \leq V_{\mathrm{DS}} < V_{\mathrm{DSAT}}$, $V_{\mathrm{GS}} \geq V_{\mathrm{T}}$ and the effective W/L ratio is given by, [108],

$$\left[\frac{W}{L}\right]_{\mathrm{eff}} = 2n\frac{\tan\left(\frac{\pi}{n}\right)}{\ln\left(\frac{W_1}{W_2}\right)} \tag{5.4}$$

The rest of the parameters are enumerated below

$$V_{\mathrm{W}} = \frac{qN_{\mathrm{A}}W_{\mathrm{T}}}{C_{\mathrm{ox}}} \tag{5.5}$$

$$W_{\mathrm{T}} = \left[\frac{2K_{\mathrm{s}}\varepsilon_0}{qN_{\mathrm{A}}}(2\phi_{\mathrm{F}})\right]^{1/2} \tag{5.6}$$

μ	carrier mobility;
C_{ox}	total oxide capacitance per unit area;
K_{s}	silicon dielectric constant;
ε_0	vacuum permittivity;
N_{A}	doping concentration;
ϕ_{F}	Fermi potential;
V_{GS}, V_{DS}	gate and drain to source voltages, respectively;
V_{TH}	threshold voltage.

In the saturation region of operation, it is necessary to estimate the length of the saturation region, that is, the extension of the channel length modulation defined through the parameter y_{ld} in Fig 5.3(b). As the precise value of y_{ld} cannot be directly extracted from measurement

data, the surface channel potential predicted by the model was compared with device simulation results using Sentaurus from Synopsys [109]. Then, the current in the saturation region is approximated by, [110],

$$I_D(V_{DS}) = \frac{I_D(V'_{DS})}{1 - \frac{y_{ld}}{L_{eq}(V'_{DS})}}, \qquad V_{DS} \geq V_{DSAT} \qquad \text{and} \qquad V_{DS} > V'_{DS} \tag{5.7}$$

where V_{DSAT} is the drain to source voltage at the saturation point and

$$L_{eq}(V'_{DS}) = L\left(1 + \frac{V'_{DS}}{LE_{sat}}\right) \tag{5.8}$$

This model was also implemented in Verilog-AMS and the code is given in Appendix C. Then, an ELT was simulated under different bias conditions to obtain its characteristic I–V curves.

5.2 Integration of Verilog-AMS language into Cadence framework

There are many CAD tools that support Verilog or VHDL cell implementation, but few that support the AMS extension and also allow the use of these cells in combination with other devices described in HSpice or Spectre. Cadence Virtuoso AMS-Designer is one of these tools which also allows the simulation of mixed-signal designs. The simulator uses Spectre and NC-Verilog to simulate the analog and digital parts respectively. Another mixed-signal simulator available in Cadence is SpectreVerilog, but only AMS-Designer can handle Verilog-AMS code. Besides, SpectreVerilog uses the same waveform viewer as Spectre, which is designed for displaying analog data, while AMS-Designer uses SimVision to plot the output waveforms. SimVision is able to plot analog and digital data much clearer than the Spectre waveform viewer. To the best of our experience, AMS-Designer is still an immature tool which is under continuous development, not as easily used as the simulators that are dedicated to either analog or digital simulation. Therefore, a short description of the necessary steps to perform the simulations related to the Verilog-AMS implementations described in the previous section seems appropriate.

The description of the following procedure is based on circuit simulations under Cadence 5.1.4 CDB, using AMS-Designer 5.1, Schematic Editor 5.10 and SimVision 9.20. Before using AMS-Designer, a file named “hdl.var” should be created in the directory where Cadence

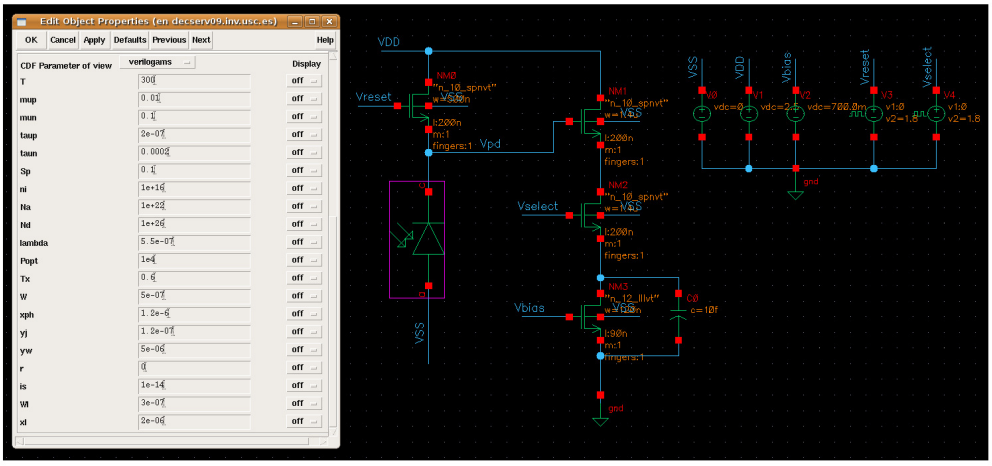


Figure 5.4: Screen capture of the 3T-APS circuit simulation showing the parameters in the Verilog-AMS model of the photodiode which can be modified.

is launched. Firstly, a new library and a new Verilog-AMS cellview must be created and then, a symbol for the cellview is generated if no errors are found. Secondly, a schematic cellview is created using Virtuoso Schematic Editor. The Verilog-AMS cells are placed as usual. The designer can modify the value of the parameters in the Verilog-AMS model from the "Edit object properties" window, as shown in the screen capture of the 3T-APS circuit simulation in Figure 5.4.

Since AMS-Designer must be operated through the Cadence hierarchy design editor, a config view must be created for the cell in order to simulate the schematic cellview. After that, a "New Configuration" pop-up appears. The "Use Template…" button is selected and "AMS" should be chosen. Then, the view must be changed to "schematic", and the library name of the design must be entered in the library list. The hierarchy editor window is opened but it is necessary to close this window along with the schematic, and then reopen the config view and select "yes" for both options.

The hierarchy editor along with the schematic should now be opened. First, the view to use for each cell in the design must be selected in the hierarchy editor and then an update is needed. Next, the AMS plug-in must be installed in order to use the AMS-Designer. As a result, the AMS dropdown menu is included at the top of the hierarchy editor. Before using the AMS simulator, a directory where to run the simulation must be chosen. In addition, the

compiler and simulator options must be configured. The next step is to compile all the files in the design and the "Design Prep" should give an output window with no errors. Finally, the signals to be plotted must be selected before running the simulation. It is important to note that SimVision will not allow the user to plot any signals which were not selected before simulation run. If the simulation is successfully run, the SimVision environment, which consists of a console, a design browser, and a waveform viewer, should start up. From the waveform viewer, the simulation run must be started and finally the output is shown in the waveform viewer.

5.3 Results

5.3.1 p-n$^+$ junction photodiode

A 3T-APS cell was simulated in Cadence framework. The proposed model in Equation (4.44) was implemented in Verilog-AMS to simulate a $x_{\text{ph}}^2 = 1.54$ μm^2 squared photodiode in a

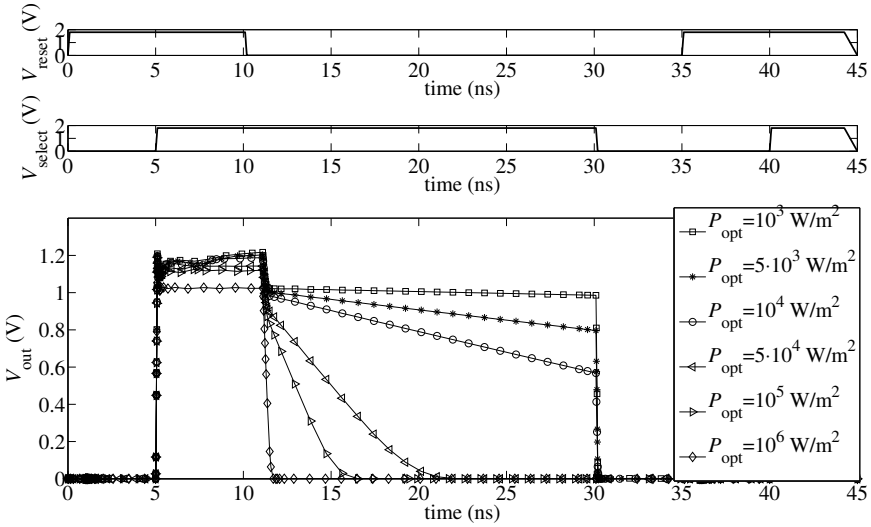
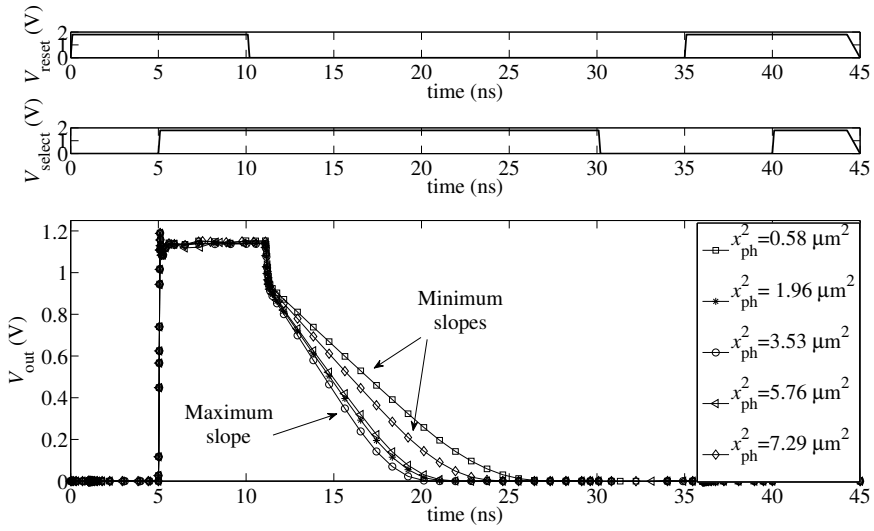
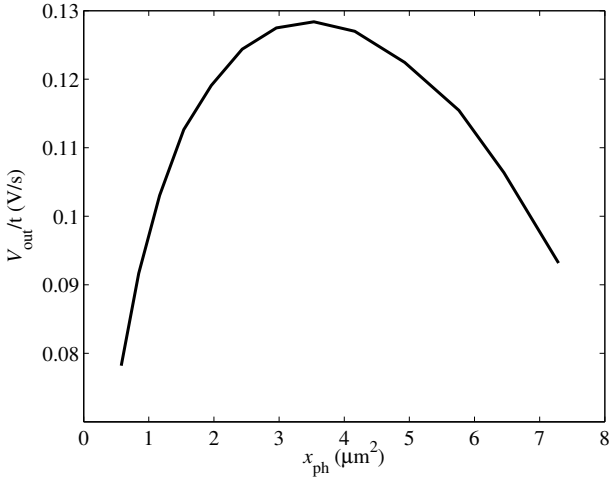


Figure 5.5: Circuit simulation results of the 3T-APS with $\lambda = 550$ nm and $x_{\text{ph}}^2 = 1.54$ μm^2. Output voltage versus time for different P_{opt} values in the integration mode operation regime.



(a) Output voltage versus time for different x_{ph}^2 values and constant x_ℓ^2 in the integration mode operation regime.



(b) Photoresponse versus the photodiode active area.

Figure 5.6: Circuit simulation results of the 3T-APS with $\lambda = 550$ nm and $P_{\text{opt}} = 5 \cdot 10^4 \text{W/m}^2$.

90 nm technology. Transistors in the library of UMC 90 nm standard technology were used to design the electronics of the pixel.

The pixel was simulated under a light source of $\lambda = 550$ nm and different values of the optical power, P_{opt}, Figure 5.5. The voltage at the output node, $V_{out}(t)$, drops from a reset value when the reset transistor is opened and the select transistor is on, as expected from Equation (5.1). As explained in Section 2.1, the slope of these decay curves permit us to determine the sensitivity of the photodetector for a given light wavelength and intensity. Being able to do this kind of characterization prior to manufacture implies a tremendous advantage as it saves important amounts of time and money.

Given the proposed model, the power operation range can be also characterized. As can be seen, there is a minimum optical power under which the pixel is not sensitive enough to the light and a very small photocurrent is generated. Consequently, the output node remains at reset voltage as is shown by the curve for $P_{opt} = 10^3$ W/m^2. In a similar way, there is an upper power limit from which the light produces a huge increase of the photocurrent. As a result, the output voltage drops dramatically as shown in the curve for $P_{opt} = 10^6$ W/m^2. This permits an a priori estimation of the dynamic range prior to fabrication with the obvious benefits implied.

In addition, the Verilog-AMS model permits to characterize the trade-off between the active and the surrounding collecting areas in terms of collection efficiency, particularly for very small photodiodes. To this aim, circuit simulations with the same photodiode total area x_ℓ^2 and different values of the active area x_{ph}^2 were performed under a light source with $P_{opt} = 5 \cdot 10^4$ W/m^2 and $\lambda = 550$ nm, Figure 5.6(a). As can be observed, even for a fixed total area, different active area sizes correspond to different pixel sensitivities given by the slope of the curve. The $V_{out}(t)$ curve with the maximum slope represents the best photodiode response, which does not correspond with the maximum size of the n^+ diffusion x_{ph}^2, Figure 5.6(b). Consequently, the results confirm that there is an optimum active area which maximizes the rate of decay of V_{out} and hence the pixel response when the lateral effects are taken into consideration, Figure 5.6(b).

Regarding the logarithmic APS, the behaviour described by Equation (5.2) was also demonstrated by means of circuit level simulations. As the photocurrent is directly proportional to the optical power P_{opt}, simulations for different values of P_{opt} were carried out. It can be observed from the circuit simulation results in the semi-log plot depicted in Figure 5.7 that the voltage on the photodiode V_{PD} is logarithmically proportional to the incident optical power.

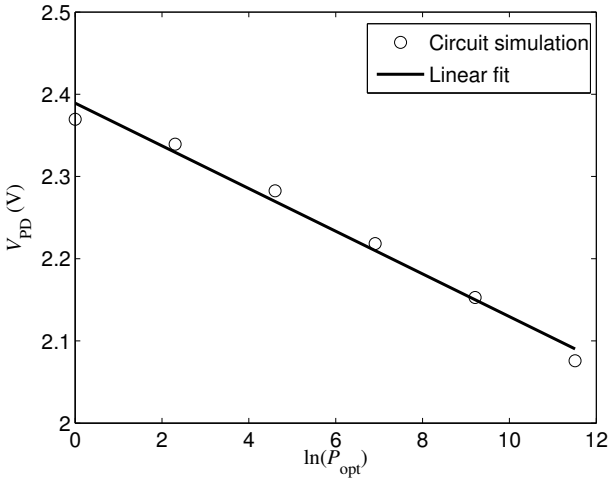


Figure 5.7: Semi-log plot of the photodiode voltage versus input optical power in logarithmic mode operation regime. The logarithmic APS was simulated for an incident radiation with $\lambda = 550$ nm.

Specifically, the equation for the linear fit is

$$V_{\mathrm{PD}} = 2.39 - 0.026 \ln\left(P_{\mathrm{opt}}\right) \tag{5.9}$$

If the previous equation is compared with Equation (5.2),

$$\begin{aligned} P_{\mathrm{s}} &= e^{\frac{q}{KT}(2.39 - V_{\mathrm{DD}})} \\ \frac{kT}{q} &= 0.026\,\mathrm{V} \end{aligned} \tag{5.10}$$

where P_{s} is the power related to the inverse-bias saturation current and KT/q matches up to the thermal voltage at room temperature. Moreover, it was proved that the logarithmic configuration is more suitable for low light intensity than the 3T-APS, covering three orders of magnitude more (from 1 to 10^5 W/m^2), although the output voltage swing is smaller.

5.3.2 Gate-Enclosed Layout Transistors (ELTs)

The circuit simulation I–V curves of an ELT with $n = 8$, $L = 0.2$ µm and $[W/L]_{\mathrm{eff}} = 15$ described in Verilog-AMS are validated with the space-charge analytical model and the measurements of an ELT transistor fabricated in a commercial CMOS 0.18 µm process, Figure 5.8.

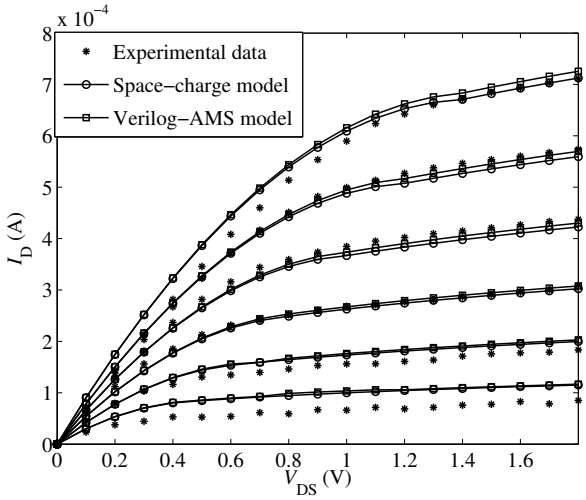


Figure 5.8: Comparison of the I–V curves of an ELT device with $n = 8$, $L = 0.2$ µm and $[W/L]_{\text{eff}} = 15$, given by the space-charge and Verilog-A models with experimental data from a CMOS 0.18 µm process.

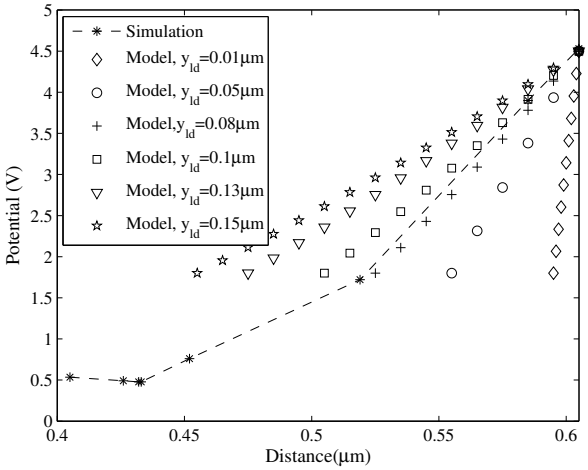


Figure 5.9: Estimation of the of the surface channel potential by comparison of the model prediction for different values of y_{ld} with device simulation.

In all cases, the drain was taken as the inner diffusion. Furthermore, the length of the saturation region, that is, the extension of the channel length modulation defined in the proposed model through the parameter y_{ld}, Figure 5.3(b), was estimated for each value of V_{GS}. As the precise value of y_{ld} cannot be directly extracted from measurement data, the surface channel potential given by the model in Equation (30), [53], was compared with device simulation results using Sentaurus from Synopsys. Figure 5.9 shows, marked with a dashed line, the resulting potential along the channel as obtained from device simulation. Also shown in this figure are the different channel potential distributions obtained applying the model for different values of y_{ld}. As can be seen, the best fit, which in this case corresponds to a value of $y_{ld} = 0.008$ μm, is taken and used in Equation (5.7) to obtain the current in saturation. As a result and as can be appreciated in Figure 5.8, both the model and its implementation in Verilog-AMS show close agreement with the experimental data.

5.4 Conclusions

In the previous chapter, a scalable analytical model for the photoresponse estimation of p-n$^+$ junctions was developed and validated through simulation and experimental results. In this chapter, the model was successfully implemented in Verilog-AMS in Cadence framework. In addition, the contribution with device simulations to the development of an analytical model for Enclosed Layout Transistors (ELTs) was used to implement this model in Verilog-AMS. A short description of the procedure with regard to the CAD tool was included as a guide for circuit simulations including such Verilog-AMS cells in Cadence framework.

The implementation of these models was validated by circuit simulation and they proved to be a valuable and powerful tool to the description of the p-n$^+$ junctions and ELTs behaviour from a designer's point of view.

Conclusions and future work

This work is focused on the study of the behaviour of small photodetectors. A total of four chips in 180 nm, 90 nm and 65 nm technological nodes were fabricated and tested to characterize different structures. The study was carried out with the aid of device simulation as well. As a result, several models were proposed and validated, which describe the photoresponse of p-n junctions with excellent agreement including lateral effects. A compact, general and scalable analytical model was also proposed and successfully implemented in Verilog-AMS.

The following conclusions summarize this work:

- Experimental measurements of 3T-APS cells with octagonal p-n^+ and square p-N_{well} junction photodiodes in UMC 180 nm CIS and UMC 90 nm standard technologies, respectively, showed the dependence of the sensitivity on the active-to-peripheral collection areas ratio. The physical phenomena in the surroundings of the junction were modelled by a semianalytical model, which fitted the experimental data with high accuracy. This fact denoted a correct understanding of the physics of the device and revealed the importance of the peripheral collection in small photodiodes. Thus, the trend towards maximizing the active area of the photodetector in order to obtain the highest photoresponse must be revised.

- An experimental sub-pixel study allowed the characterization of the photoresponse of the different regions of the pixel. In this way, 3T-APS cells with square p-n^+ and p-N_{well} junction photodiodes in UMC 90 nm standard technology were scanned and measured in terms of photocurrent by means of a point source illumination. These structures were modelled by an analytical solution of the steady-state equation in the different regions of the pixel. Both the model and the experimental data showed an important photoresponse due to the illumination of the collecting area surrounding the

junction. In addition, device simulations of a p-n^+ junction with different values of the active area and constant total size were done. Only the surroundings of the junction were exposed to the uniform light source, showing a trade-off between the active and peripheral collecting areas which optimized the response and the predominance of the peripheral photoresponse over the active area response.

– An analytical model of the lateral photoresponse based on the solution of the two-dimensional steady-state equation was proposed and fitted with excellent agreement the device simulation results. The predictions were validated with experimental measurements of square p-n^+ junction photodiodes in AMS 180 nm and UMC 65 nm standard technologies. Photodiodes with different values of the diffusion and the collecting area surrounding the junction were measured under uniform illumination. The same structures with an optical shield over the active area were also measured in the same conditions to characterize the peripheral photoresponse. The experimental data confirmed the behaviour predicted by the device simulations and the proposed model reproduced the response of the structures in both technologies. As a result, a general, scalable and compact model for CMOS photodiodes operated in the visible range was obtained. Its validity in deep sub-micron CMOS processes was experimentally demonstrated.

– The proposed model was implemented in a hardware description language and used for circuit simulation purposes. It constitutes a powerful tool which can be used to aid the design of CMOS imagers in computer aided design tools.

– The potential of having a Verilog-AMS implementation of non-standard CMOS devices such as ELT transistors in conventional CAD tools was also demonstrated.

The research line remains open, as the following points should be explored:

– Spectral response characterization of the p-n^+ junctions in AMS 180 nm and UMC 65 nm standard technologies in the visible range. Despite not being essential for this work, a through characterization of the fabricated photodiodes with different values of the light source wavelength is desirable and will be attempted in the near term.

– Fabrication and characterization of different junctions, such us p-N_{well} and pinned photodiodes. As the model is expected to be easily extended to other photodetector structures and geometries with minor changes, different junctions should be fabricated in order to validate the model for each case.

– Crosstalk characterization and modelling. Despite its dependence on the pixels arrangement for each particular design, a crosstalk model is desirable as pixel size shrinks. In this way, arrays of photodiodes with different neighbourhood orders will be characterized in the near future.

– Exploration of technological nodes beyond 65 nm. It is essential to characterize CMOS photodetectors in deep sub-micron and nano technologies for the purpose of determining the scaling limit of pixel dimensions and the viability of implementations in advanced technological nodes. Moreover, the analytical model proposed in this work could be modified to consider additional phenomena, such as quantum effects, if needed. However, the main determining factor to carry out these goals is the fabrication cost of advanced technologies.

– Noise modelling. The different sources of noise can be included in the photodiode model to perform more accurate circuit simulations when required by the design. An in-depth study of the noise models in the literature is necessary in order to state their validity in advanced technologies.

APPENDIX A

NOMENCLATURE AND SYMBOLS

	Symbol	Value	Units
Speed of light in vacuum	c	$3 \cdot 10^{8}$	m/s
Vacuum permittivity	ε_0	$8.85 \cdot 10^{-12}$	F/m
Planck's constant	h	$6.63 \cdot 10^{-34}$	Js
Boltzmann constant	K	$8.617 \cdot 10^{-5}$	eV/K
Silicon dielectric constant	K_s	11.68	-
Intrinsic carrier concentration (Si, T)	n_i	$1 \cdot 10^{16}$	m^{-3}
Electron charge	q	$1.6 \cdot 10^{-19}$	C
Room temperature	T	300	K

Table A.1: Physical constants.

	Symbol	Units
Absorption coefficient	α	m^{-1}
Active area apothem	a	m
Apothem of the inner diffusion	$a_{p,i}$	m
Photodetector junction area	A	m^2
Pixel area	A_{pix}	m^2
Point source area	A_{ps}	m^2
Photodetector side-walls areas	A_P	m^2
Fitting parameter	γ	m^{-4}
Unit junction bottom area capacitance	C_A	F/m^2
Conversion gain	CG	V/e^-

Table A.2: List of symbols.

	Symbol	Units
Unit zero-bias junction bottom area capacitance	C_{JO}	F/m^2
Unit zero-bias junction side-wall capacitance	C_{JOP}	F/m^2
Unit junction side-wall capacitance	C_{P}	F/m^2
Photodetector capacitance	C_{PD}	F
Depletion region depth	d	µm
Electron diffusion coefficient	D_{n}	m^2/s
Hole diffusion coefficient	D_{p}	m^2/s
Dynamic range	DR	dB
Extension of the outer diffusion over the gate	E	m
Semiconductor band gap energy	E_{g}	eV
Fill factor	FF	%
Optical generation rate	G	1/s m^3
Charge collection efficiency	η	-
Current	I	A
Active area photocurrent	I_{aa}	A
Lateral photocurrent	I_{lateral}	A
Lateral depletion region photocurrent	I_{W}	A
Current density	J	A/m^2
Photocurrent density	J_{ph}	A/m^2
Light wavelength	λ	m
Square side of the well	l	m
Square side of the diffusion	l_{diff}	m
Square side of the point source	l_{ps}	m
Channel length of the transistor	L	m
Electron diffusion length	L_{diff}, L_{n}	m
Hole diffusion length	L_{p}	m
Electron mobility	μ_{n}	m^2/V s
Hole mobility	μ_{p}	m^2/V s
Junction grading coefficient of the bottom area	M_{J}	-
Junction grading coefficient of the side-walls	M_{JP}	-
Modulation Transfer Function	MTF	-
Light frequency	ν	Hz
Electron concentration	n_{p}	m^{-3}
Equilibrium electron concentration	n_{p0}	m^{-3}
Electron excess concentration	N	m^{-3}
Acceptor concentration	N_{A}	m^{-3}
Donor concentration	N_{D}	m^{-3}
Full-well capacity	N_{sat}	m^{-3}

Table A.2: List of symbols (*continued from previous page*).

	Symbol	Units
Generated signal charge	N_{sig}	m^{-3}
Hole concentration	p_{n}	m^{-3}
Equilibrium hole concentration	p_{n0}	m^{-3}
Active area perimeter	P	m
Incident optical power	P_{opt}	W/m^2
Quantum efficiency	QE	%
Responsivity	R	$\text{e}^-/\text{s lux}$
Reflection coefficient	R_{c}	-
Sensitivity	S	V/s lux
Surface recombination velocity of electrons	S_{n}	m/s
Surface recombination velocity of holes	S_{p}	m/s
Signal-to-noise ratio	SNR	dB
Electron lifetime	τ_{n}	s
Hole lifetime	τ_{p}	s
Integration time	t_{int}	s
Transmission coefficient	T_{c}	%
Drain to source voltage	V_{DS}	V
Gate to source voltage	V_{GS}	V
Photodetector bias voltage	V_{PD}	V
Threshold voltage	V_{TH}	V
Built-in potential of the bottom area	ϕ_{B}	V
Built-in potential of the side-walls	ϕ_{BP}	V
Fermi potential	ϕ_{F}	V
Photon flux	Φ	$1/\text{s m}^2$
Photon flux at the surface	Φ_0	$1/\text{s m}^2$
Vertical depletion region thickness	W	m
Sides of the source, gate and drain	$W_{1,2,3}$	m
Lateral depletion region thickness	W_ℓ	m
Device width	x_ℓ	m
Diffusion width	x_{ph}	m
Well width	x_{well}	m
Junction depth	y_{j}	m
Saturation region length	y_{ld}	m
Diffusion depth (p-N_{well})	y_{ph}	m
Device thickness	y_{w}	m

Table A.2: List of symbols (*continued from previous page*).

APPENDIX B

MODELS PARAMETERS

Semianalytical model

Parameters used for the validation of the semianalytical model:

	Symbol	Value	Units
Depletion region depth	d	0.1	µm
Diffusion length of the photocarriers (electrons)	L_{diff}	1	µm
Unit zero-bias junction bottom area capacitance	C_{JO}	$9.65 \cdot 10^{-16}$	F/m^2
Unit zero-bias junction peripheral capacitance	dC_{JOP}	$1.70 \cdot 10^{-16}$	F/m
Photodetector bias voltage	V_{PD}	0.6	V
Built-in potential of the bottom area	ϕ_{B}	0.80	V
Built-in potential of the side-walls	ϕ_{BP}	0.65	V
Junction grading coefficient of the bottom area	M_{J}	0.41	-
Junction grading coefficient of the side-walls	M_{JP}	0.35	-

Table B.1: 180 nm technology.

	Symbol	Value	Units
Depletion region depth	d	0.5	µm
Diffusion length of the photocarriers (electrons)	L_{diff}	1	µm
Unit zero-bias junction bottom area capacitance	C_{JO}	$8.76 \cdot 10^{-16}$	F
Unit zero-bias junction peripheral capacitance	dC_{JOP}	$3.20 \cdot 10^{-17}$	F
Photodetector bias voltage	V_{PD}	0.3	V
Built-in potential of the bottom area	ϕ_{B}	0.60	V
Built-in potential of the side-walls	ϕ_{BP}	0.31	V
Junction grading coefficient of the bottom area	M_{J}	0.25	-
Junction grading coefficient of the side-walls	M_{JP}	$1 \cdot 10^{-5}$	-

Table B.2: 90 nm technology.

Coefficient of multiple determination of the proposed semianalytical model fitted to experimental data:

$f_1 = 0.50A$	$f_1 = 0.75A$	$f_1 = A$	$f_2 = \log_{10}\left(1 + \frac{\ell}{L_{\text{diff}}}\right)$
0.9490	0.8861	0.8312	0.9428

Table B.3: p-n$^+$ photodiodes.

	$f_1 = 0.50A$	$f_1 = 0.75A$	$f_1 = A$	$f_2 = \log_{10}\left(1 + \frac{\ell}{L_{\text{diff}}}\right)$
$R_{\text{A1}} = C_1 A_{\text{diff}}$	-	-	-	-
$R_{\text{A2}} = C_1 A$	0.8346	0.8480	0.8584	0.8312
$R_{\text{A3}} = C_1 \frac{l_{\text{diff}}}{l} A$	0.6969	0.5985	0.5037	0.7144
$R_{\text{A4}} = C_1 A^{l_{\text{diff}}/l}$	0.9310	0.9204	0.8541	0.9160

Table B.4: p-N$_{\text{well}}$ photodiodes with $l_{\text{diff}} = 0.80$ µm

	$f_1 = 0.50A$	$f_1 = 0.75A$	$f_1 = A$	$f_2 = \log_{10}\left(1 + \frac{\ell}{L_{\text{diff}}}\right)$
$R_{\text{A1}} = C_1 A_{\text{diff}}$	0.3115	0.1705	0.0526	0.2343
$R_{\text{A2}} = C_1 A$	0.9257	0.9318	0.9363	0.9295
$R_{\text{A3}} = C_1 \frac{l_{\text{diff}}}{l} A$	0.9157	0.9029	0.8924	0.9081
$R_{\text{A4}} = C_1 A^{l_{\text{diff}}/l}$	0.9445	0.9219	0.9002	0.9305

Table B.5: p-N$_{\text{well}}$ photodiodes with $l_{\text{diff}} = 1.28$ µm

	$f_1 = 0.50A$	$f_1 = 0.75A$	$f_1 = A$	$f_2 = \log_{10}\left(1 + \frac{\ell}{L_{\text{diff}}}\right)$
$R_{\text{A1}} = C_1 A_{\text{diff}}$	0.6064	0.5755	0.5514	0.5820
$R_{\text{A2}} = C_1 A$	0.7998	0.8070	0.8124	0.8057
$R_{\text{A3}} = C_1 \frac{l_{\text{diff}}}{l} A$	0.7973	0.7930	0.7777	0.7938
$R_{\text{A4}} = C_1 A^{l_{\text{diff}}/l}$	0.8216	0.8076	0.7965	0.8102

Table B.6: p-N_{well} photodiodes with $l_{\text{diff}} = 1.52$ µm

	$f_1 = 0.50A$	$f_1 = 0.75A$	$f_1 = A$	$f_2 = \log_{10}\left(1 + \frac{\ell}{L_{\text{diff}}}\right)$
$R_{\text{A1}} = C_1 A_{\text{diff}}$	0.9856	0.9857	0.9857	0.9857
$R_{\text{A2}} = C_1 A$	0.9806	0.9794	0.9786	0.9792
$R_{\text{A3}} = C_1 \frac{l_{\text{diff}}}{l} A$	0.9802	0.9796	0.9792	0.9795
$R_{\text{A4}} = C_1 A^{l_{\text{diff}}/l}$	0.9789	0.9789	0.9789	0.9789

Table B.7: p-N_{well} photodiodes with $l_{\text{diff}} = 2.00$ µm

Analytical model: point source illumination

Parameters used for the validation of the analytical model using a point source illumination:

	Symbol	Value	Units
Electron mobility	μ_n	$100 \cdot 10^{-3}$	$m^2/V\,s$
Hole mobility	μ_p	$10 \cdot 10^{-3}$	$m^2/V\,s$
Electron diffusion coefficient	D_n	$2.6 \cdot 10^{-3}$	m^2/s
Hole diffusion coefficient	D_p	$2.6 \cdot 10^{-4}$	m^2/s
Electron lifetime	τ_n	$200 \cdot 10^{-6}$	s
Hole lifetime	τ_p	$0.2 \cdot 10^{-6}$	s
Electron diffusion length	L_n	$7.21 \cdot 10^{-4}$	m
Hole diffusion length	L_p	$7.21 \cdot 10^{-6}$	m
Surface recombination velocity of electrons	S_n	50	m/s
Surface recombination velocity of holes	S_p	0.1	m/s
Acceptor concentration	N_A	$1 \cdot 10^{22}$	m^{-3}
Donor concentration	N_D	$1 \cdot 10^{26}$	m^{-3}
Equilibrium electron concentration	n_{p0}	$1 \cdot 10^{10}$	m^{-3}
Equilibrium hole concentration	p_{n0}	$1 \cdot 10^{6}$	m^{-3}
Depletion region thickness (in y-direction)	W	$0.50 \cdot 10^{-6}$	m
Depletion region thickness (in x-direction)	W_ℓ	$0.30 \cdot 10^{-6}$	m
Junction depth	y_j	$0.12 \cdot 10^{-6}$	m
Device thickness	y_w	$5 \cdot 10^{-6}$	m
Transmission coefficient	T_c	0.6	-
Incident optical power	P_{opt}	175000	W/m^2

Table B.8: p-n$^+$ junction photodiodes under point source illumination in 90 nm technology.

	Symbol	Value	Units
Electron mobility	μ_{n}	$100 \cdot 10^{-3}$	$\mathrm{m^2/V\,s}$
Hole mobility	μ_{p}	$10 \cdot 10^{-3}$	$\mathrm{m^2/V\,s}$
Hole mobility (well)	μ_{p2}	0.03	$\mathrm{m^2/Vs}$
Electron diffusion coefficient	D_{n}	$2.6 \cdot 10^{-3}$	$\mathrm{m^2/s}$
Hole diffusion coefficient (diffusion)	D_{p1}	$2.6 \cdot 10^{-4}$	$\mathrm{m^2/s}$
Hole diffusion coefficient (well)	D_{p2}	$7.8 \cdot 10^{-4}$	$\mathrm{m^2/s}$
Electron lifetime	τ_{n}	$200 \cdot 10^{-6}$	s
Hole lifetime	τ_{p}	$0.2 \cdot 10^{-6}$	s
Electron diffusion length	L_{n}	$7.21 \cdot 10^{-4}$	m
Hole diffusion length (diffusion)	L_{p1}	$7.21 \cdot 10^{-6}$	m
Hole diffusion length (well)	L_{p2}	$1.25 \cdot 10^{-5}$	m
Surface recombination velocity of electrons	S_{n}	50	m/s
Surface recombination velocity of holes	S_{p}	0.1	m/s
Acceptor concentration	N_{A}	$1 \cdot 10^{22}$	$\mathrm{m^{-3}}$
Donor concentration (diffusion)	N_{D1}	$1 \cdot 10^{24}$	$\mathrm{m^{-3}}$
Donor concentration (well)	N_{D2}	$1 \cdot 10^{26}$	$\mathrm{m^{-3}}$
Equilibrium electron concentration	n_{p0}	$1 \cdot 10^{10}$	$\mathrm{m^{-3}}$
Equilibrium hole concentration (diffusion)	p_{n01}	$1 \cdot 10^{8}$	$\mathrm{m^{-3}}$
Equilibrium hole concentration (well)	p_{n02}	$1 \cdot 10^{6}$	$\mathrm{m^{-3}}$
Depletion region thickness (in y-direction)	W	$0.35 \cdot 10^{-6}$	m
Depletion region thickness (in x-direction)	W_{ℓ}	$0.25 \cdot 10^{-6}$	m
Diffusion depth	y_{ph}	$0.12 \cdot 10^{-6}$	m
Junction depth	y_{j}	$0.20 \cdot 10^{-6}$	m
Device thickness	y_{w}	$5 \cdot 10^{-6}$	m
Transmission coefficient	T_{c}	0.6	-
Incident optical power	P_{opt}	175000	$\mathrm{W/m^2}$

Table B.9: p-$\mathrm{N_{well}}$ junction photodiodes under point source illumination in 90 nm technology.

Analytical model: uniform illumination

Parameters used for the validation of the analytical model for p-n$^+$ junction photodiodes under uniform illumination:

	Symbol	Value	Units
Electron mobility	μ_n	$100 \cdot 10^{-3}$	$m^2/V\,s$
Hole mobility	μ_p	$10 \cdot 10^{-3}$	$m^2/V\,s$
Electron diffusion coefficient	D_n	$2.6 \cdot 10^{-3}$	m^2/s
Hole diffusion coefficient	D_p	$2.6 \cdot 10^{-4}$	m^2/s
Electron lifetime	τ_n	$200 \cdot 10^{-6}$	s
Hole lifetime	τ_p	$0.2 \cdot 10^{-6}$	s
Electron diffusion length	L_n	$7.21 \cdot 10^{-4}$	m
Hole diffusion length	L_p	$7.21 \cdot 10^{-6}$	m
Surface recombination velocity of holes	S_p	0.1	m/s
Acceptor concentration	N_A	$1 \cdot 10^{22}$	m^{-3}
Donor concentration	N_D	$1 \cdot 10^{26}$	m^{-3}
Equilibrium electron concentration	n_{p0}	$1 \cdot 10^{10}$	m^{-3}
Equilibrium hole concentration	p_{n0}	$1 \cdot 10^{6}$	m^{-3}
Depletion region thickness (in y-direction)	W	$0.50 \cdot 10^{-6}$	m
Depletion region thickness (in x-direction)	W_ℓ	$0.30 \cdot 10^{-6}$	m
Junction depth	y_j	$0.12 \cdot 10^{-6}$	m
Device thickness	y_w	$5 \cdot 10^{-6}$	m
Transmission coefficient	T_c	0.6	-

Table B.10: 90 nm technology.

	Symbol	Value	Units
Electron mobility	μ_{n}	$31.7 \cdot 10^{-3}$	$\mathrm{m^2/V\,s}$
Hole mobility	μ_{p}	$7 \cdot 10^{-3}$	$\mathrm{m^2/V\,s}$
Electron diffusion coefficient	D_{n}	$8.24 \cdot 10^{-4}$	$\mathrm{m^2/s}$
Hole diffusion coefficient	D_{p}	$1.82 \cdot 10^{-4}$	$\mathrm{m^2/s}$
Electron lifetime	τ_{n}	$200 \cdot 10^{-6}$	s
Hole lifetime	τ_{p}	$0.2 \cdot 10^{-6}$	s
Electron diffusion length	L_{n}	$4.06 \cdot 10^{-4}$	m
Hole diffusion length	L_{p}	$6.03 \cdot 10^{-6}$	m
Surface recombination velocity of holes	S_{p}	0.1	m/s
Acceptor concentration	N_{A}	$1 \cdot 10^{23}$	$\mathrm{m^{-3}}$
Donor concentration	N_{D}	$1 \cdot 10^{27}$	$\mathrm{m^{-3}}$
Equilibrium electron concentration	n_{p0}	$1 \cdot 10^{9}$	$\mathrm{m^{-3}}$
Equilibrium hole concentration	p_{n0}	$1 \cdot 10^{5}$	$\mathrm{m^{-3}}$
Depletion region thickness (in y-direction)	W	$0.18 \cdot 10^{-6}$	m
Depletion region thickness (in x-direction)	W_{ℓ}	$0.10 \cdot 10^{-6}$	m
Junction depth	y_{j}	$0.2 \cdot 10^{-6}$	m
Device thickness	y_{w}	$3 \cdot 10^{-6}$	m
Transmission coefficient	T_{c}	0.6	-

Table B.11: 180 nm technology.

	Symbol	Value	Units
Electron mobility	μ_{n}	$24 \cdot 10^{-3}$	$\mathrm{m}^2/\mathrm{V\,s}$
Hole mobility	μ_{p}	$6.8 \cdot 10^{-3}$	m^2/Vs
Electron diffusion coefficient	D_{n}	$6.24 \cdot 10^{-4}$	m^2/s
Hole diffusion coefficient	D_{p}	$1.77 \cdot 10^{-4}$	m^2/s
Electron lifetime	τ_{n}	$200 \cdot 10^{-6}$	s
Hole lifetime	τ_{p}	$0.2 \cdot 10^{-6}$	s
Electron diffusion length	L_{n}	$3.53 \cdot 10^{-4}$	m
Hole diffusion length	L_{p}	$5.95 \cdot 10^{-6}$	m
Surface recombination velocity of holes	S_{p}	0.1	m/s
Acceptor concentration	N_{A}	$2.8 \cdot 10^{23}$	m^{-3}
Donor concentration	N_{D}	$2.8 \cdot 10^{27}$	m^{-3}
Equilibrium electron concentration	n_{p0}	$3.57 \cdot 10^{8}$	m^{-3}
Equilibrium hole concentration	p_{n0}	$3.57 \cdot 10^{4}$	m^{-3}
Depletion region thickness (in y-direction)	W	$0.11 \cdot 10^{-6}$	m
Depletion region thickness (in x-direction)	W_{ℓ}	$0.05 \cdot 10^{-6}$	m
Junction depth	y_{j}	$0.1 \cdot 10^{-6}$	m
Device thickness	y_{w}	$3 \cdot 10^{-6}$	m
Transmission coefficient	T_{c}	0.6	-

Table B.12: 65 nm technology.

APPENDIX C

VERILOG-AMS CODES

p-n$^+$ junction photodiode

```
`include "constants.vams"
`include "/home/cad/disciplines.vams"

module Photodiode (a,c);

    parameter real T=300;
    parameter real mup=100e-4;
    parameter real mun=1000e-4;
    parameter real taup=0.2e-6;
    parameter real taun=200e-6;
    parameter real Sp=0.1;
    parameter real ni=1e16;
    parameter real Na=1e22;
    parameter real Nd=1e26;
    parameter real lambda=500e-9;
    parameter real Popt=1000;
    parameter real Tx=0.6;
    parameter real W=0.5e-6;
    parameter real Wl=0.3e-6;
```

```
parameter real xph=1.2e-6;
parameter real x1=4e-6;
parameter real yj=0.12e-6;
parameter real yw=5e-6;
parameter real r=0;
parameter real is=1e-14;

real alfa, ter11, ter21, ter31, ter41, ter12, ter22,
    ter32, ter42, Iaa, Iw, Ilat, Q, H, PI, velC, A, C, D,
    Jw, Jn, Jp, K, Dp, Dn, Lp, Ln, npo, pno, phi0, kp, kn,
     k, En, e1, e3, de1, de2, Cons10, Cons11, Cons20,
    Cons21, Cons3, N, dN, expn, Sn, gamma;

inout a, c;
electrical a, c;

initial begin
    PI=3.14159265358979323846;
    Q=1.602176462e-19;
    H=6.62606876e-34;
    velC=2.99792458e8;
    En=(6.2415e18*Q*velC)/lambda;
    e1=1.09969;
    e3=1.40985;
    de1=0.0583148;
    de2=0.0220161;
    Cons10=503002;
    Cons11=48391.6;
    Cons20=163430;
    Cons21=7940.79;
    Cons3=104608;
    N=0.394122;
    dN=1.23084;
```

```
        expn=N+dN*En;
    end

    analog begin
        alfa=(1/En)*((Cons10/4)*pow((En-e1-de1+abs(En-e1-de1)
            ),2)+(Cons11/4)*pow((En-e1+de1+abs(En-e1+de1)),2)
            +(Cons20/4)*pow((En-e1-de2+abs(En-e1-de2)),2)+(
            Cons21/4)*pow((En-e1+de2+abs(En-e1+de2)),2)+Cons3
            *((En-e3+abs(En-e3))**expn));

        Sn=54.5*limexp(-76470*lambda)-1.3e12*limexp(-5.359e7*
            lambda);

        gamma=35e27*lambda*Popt;
        K=8.617e-5*Q;
        Dp=0.026*mup;
        Dn=0.026*mun;
        Lp=sqrt(taup*Dp);
        Ln=sqrt(taun*Dn);
        npo=ni*ni/Na;
        pno=ni*ni/Nd;
        phi0=Popt*Tx*lambda/(H*velC);
        kp=phi0*alfa*taup/(1-alfa*alfa*Lp*Lp);
        kn=phi0*alfa*taun/(1-alfa*alfa*Ln*Ln);
        k=phi0*alfa/Dn;

        if (V(a,c) > 0)
                I(a,c) <+ 0;
        else
                A=(npo*(limexp(Q*V(a,c)/(K*T))-1)-kn*limexp
                    (-1*alfa*(yj+W)))/limexp(-1*(yj+W)/Ln);
                C=((Dp-Sp*Lp)*(pno+kp*limexp(-1*alfa*yj))+
                    limexp(yj/Lp)*kp*Lp*(Sp+alfa*Dp))/((-1*Dp+
```

```
        Sp*Lp)*limexp(-1*yj/Lp)-(Dp+Sp*Lp)*limexp(
        yj/Ln));
    D=((Dp+Sp*Lp)*(pno+kp*limexp(-1*alfa*yj))-
        limexp(-1*yj/Lp)*kp*Lp*(Sp+alfa*Dp))/((-1*
        Dp+Sp*Lp)*limexp(-1*yj/Lp)-(Dp+Sp*Lp)*
        limexp(yj/Ln));

    Jw=Q*phi0*limexp(-1*alfa*yj)*(1-limexp(-1*
        alfa*W));
    Jn=Q*Dn*(((-1*phi0*alfa*alfa*taun*limexp(-1*
        alfa*(yj+W)))/(1-alfa*alfa*Ln*Ln))-(A/Ln)*
        limexp(-1*(yj+W)/Ln));
    Jp=-1*Q*Dp*(((-1*phi0*alfa*alfa*taup*limexp
        (-1*alfa*yj))/(1-alfa*alfa*Lp*Lp))-(C/Lp)*
        limexp(-1*yj/Lp)+(D/Lp)*limexp(yj/Lp));

    ter11=(-1)*gamma*(Dn/Sn)*cosh((1/Ln)*yw)/(pow
        (1/Ln,2)+pow(PI/yw,2));
    ter21=(k/(pow((1/Ln),2)+pow(alfa,2)))*((cosh
        ((1/Ln)*yw)*limexp((-1)*alfa*yw))/(pow((1/
        Ln),2)+pow(PI/yw,2))-sinh(alfa*yw)/(pow(
        alfa,2)+pow(PI/yw,2)));
    ter31=sqrt(pow((1/Ln),2)+pow(PI/yw,2))*(1-
        cosh(sqrt(pow((1/Ln),2)+pow(PI/yw,2))*(x1
        /2-xph/2-Wl)))/sinh(sqrt(pow((1/Ln),2)+pow
        (PI/yw,2))*(x1/2-xph/2-Wl));
    ter41=(1-cos((PI/yw)*yj));

    ter12=(-1)*gamma*(Dn/Sn)*cosh((1/Ln)*yw)/(pow
        (1/Ln,2)+pow(2*PI/yw,2));
    ter22=(k/(pow(1/Ln,2)+pow(alfa,2)))*((cosh
        ((1/Ln)*yw)*limexp((-1)*alfa*yw))/(pow((1/
```

```
            Ln),2)+pow(2*PI/yw,2))-sinh(alfa*yw)/(pow(
            alfa,2)+pow(2*PI/yw,2)));
        ter32=sqrt(pow((1/Ln),2)+pow(2*PI/yw,2))*(1-
            cosh(sqrt(pow((1/Ln),2)+pow(2*PI/yw,2))*(
            x1/2-xph/2-Wl)))/sinh(sqrt(pow((1/Ln),2)+
            pow(2*PI/yw,2))*(x1/2-xph/2-Wl));
        ter42=(1-cos((2*PI/yw)*yj));

        Iaa=(Jw+Jn+Jp)*xph*xph;
        Iw=4*Q*xph*Wl*phi0*(1-limexp(-1*alfa*yj));
        Ilat=8*xph*Q*Dn/yw*((-1)*(ter11+ter21)*ter31*
            ter41+(ter12+ter22)*ter32*ter42);

        I(a,c)<+(-1)*(Iaa+Iw+Ilat);

    end
endmodule
```

Gate-enclosed layout transistor

```
`include "constants.vams"
`include "/home/cad/disciplines.vams"

module donut (d,g,s);

        parameter real T=300;
        parameter real WLeff=15;
        parameter real L=0.2e-6;
        parameter real yld=0.08e-6;
        parameter real E=3e5;
        parameter real WT=0.2e-6;
        parameter real mobility=97e-4;
        parameter real Eox=3.453e-11;
        parameter real Tox=8.3e-9;
        parameter real VT=0.05;
        parameter real NA=2e22;
        parameter real ni=1.18e16;
        parameter real step=0.1;

        real q, K, Cgox, W, Vw, PotFermi, Leq, index, u, v,
            Idstmp, sat;

        inout d,g,s;
        electrical d,g,s;

        analog begin
                q=1.6e-19;
                K=1.38e-23;
                Cgox=Eox/Tox;
                W=WLeff*L;
                Vw=q*NA*WT/Cgox;
```

```
                PotFermi=(K*T/q)*ln(NA/ni);
                sat=V(g,s)-step-V(d,s);

                if (sat > 0) begin
                        I(d,s) <+ mobility*Cgox*(W/L)*((V(g,s
                            )-VT)*V(d,s)-pow(V(d,s),2)/2-4/3*
                            Vw*PotFermi*(pow(1+(V(d,s)/(2*
                            PotFermi)),1.5)-(1+3*V(d,s)/(4*
                            PotFermi))));
                end
                else begin
                        Leq=1;
                        u = V(g,s)-2*step;
                        v = V(d,s);
                        for (index=u; index<v; index=index+
                            step)
                                Leq = Leq*(1-yld/(L*(1+(index
                                    /(L*E)))));
                        Idstmp=mobility*Cgox*(W/L)*((V(g,s)-
                            VT)*(V(g,s)-2*step)-pow((V(g,s)-2*
                            step),2)/2-4/3*Vw*PotFermi*(pow
                            (1+((V(g,s)-2*step)/(2*PotFermi))
                            ,1.5)-(1+3*(V(g,s)-2*step)/(4*
                            PotFermi))));
                        I(d,s) <+ Idstmp/Leq;
                end
        end
endmodule
```

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