Simulations of Statistical Variability in n-type FinFET, Nanowire and Nanosheet FETs

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***Abstract*—Four sources of variability, metal grain granularity (MGG), line-edge roughness (LER), gate-edge roughness (GER), and random discrete dopants (RDD), affecting the performance of state-of-the-art FinFET, nanosheet (NS), and nanowire (NW) FETs, are analysed via our in-house 3D finite-element drift-diffusion/Monte Carlo simulator that includes 2D Schrödinger equation quantum corrections. The MGG and LER are the sources of variability that influence device performance of the three multi-gate architectures the most. The FinFET and the NS FET are similarly affected by the MGG variations with threshold voltage and on-current standard deviations significantly lower (at least 20 %) than those of the NW FET. The LER variability has a negligible influence in the NS FET performance with σV_T values around 12 and 42 times lower than those of the FinFET and the NW FET. The three architectures are equally affected by the RDD (σV_T= 8 mV) and minimally influenced by the GER ($\sigma V_T \approx 4$ mV). The variability of NS FETs makes them strong candidates to replace FinFETs.**

***Index Terms*—Drift-diffusion, FinFET, Nanosheet, Nanowire, Monte Carlo, Schrödinger Quantum Correction, Variability.**

I. Introduction

FINFET architecture has been dominant for digital applications during the last years [1]. However, a changeover will be needed for future CMOS technology generations in order to maintain a good electrostatic control [2]. Gate-all-around (GAA) nanowire (NW) FETs are currently considered as one of the strongest contenders to replace the FinFETs because of their superior gate control [3] but, their adoption implies a substantial change in the fabrication processes [4]. The GAA nanosheet (NS) FETs have been proposed as an intermediate step between both architectures due to a slightly better performance than the FinFETs [5] while reusing, with minimal changes [6], its fabrication process.

The continuous scaling of device dimensions brought an increase in process induced variability. The main variability sources affecting the reliability of multi-gate transistors are: metal-gate work-function granularity (MGG), line edge roughness (LER), gate edge roughness (GER), random discrete dopants (RDD), oxide thickness variation (OTV), and interface trap charges (ITC) [7]. The minimisation of this device variability is essential to reduce further a supply voltage and thus a power dissipation [8]. The impact of variability in multi-gate transistor architectures [9], [10], [11], [12] has been intensively analysed but, to our best knowledge, no thorough studies exist that would compare a variability of nanoscale FinFET, NS and NW FET architectures. Therefore, in this work, we investigate the effect that four different sources of variability (MGG, LER, GER and RDD) have on the performance of realistic, Si-based FinFET, NW FET, and NS FET. VENDES [13], an in-house-built 3D finite-element physically-based simulation toolbox, is used to analyse the variability effect on the devices performance. VENDES combines quantum-corrected drift-diffusion and ensemble Monte Carlo transport models via the 2D Schrödinger equation to precisely model both sub-threshold and on-region device characteristics.

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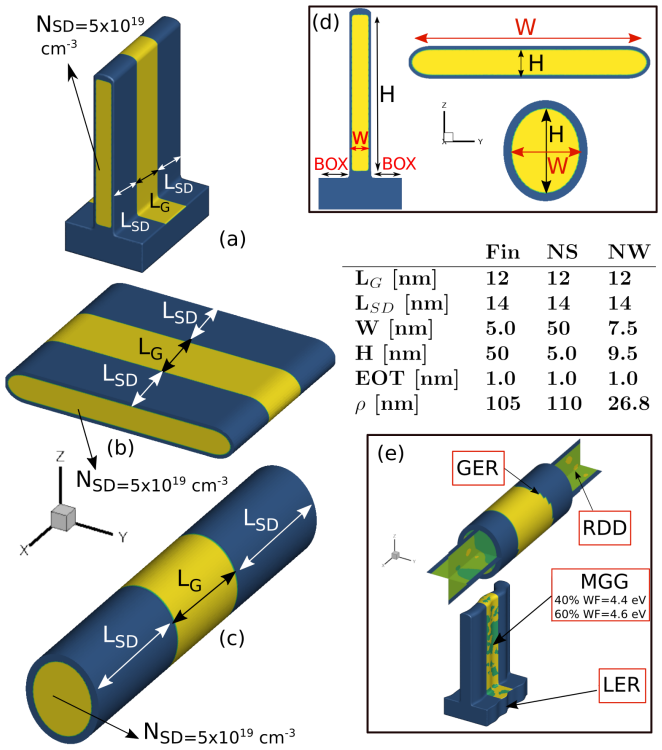

	Fin	NS	NW
L_G [nm]	12	12	12
L_{SD} [nm]	14	14	14
W [nm]	5.0	50	7.5
H [nm]	50	5.0	9.5
EOT [nm]	1.0	1.0	1.0
ρ [nm]	105	110	26.8

Figure 1. 3D schemes of the FinFET (a), NS FET (b), and NW FET (c). 2D schemes of their respective cross-sections are shown in (d). The device dimensions: physical gate (L_G), source/drain lengths (L_{SD}), channel width (W) and height (H), effective oxide thickness (EOT), and semiconductor perimeter (ρ), are included in a table. The devices have an uniform p-type doping (1.0×10^{15} cm^{-3}) in the channel and a n-type Gaussian doping in the S/D regions (N_{SD}). (e) Examples of devices affected by GER, RDD, MGG and LER variability.

II. 3D Modelling of Variability

Figs. 1(a)-(c) present 3D schemes of the three device architectures and show their physical dimensions. The 12 nm NS FET structure is designed after the experimental device reported in [6] and it was previously validated in [5]. Because doping profiles in the source/drain and channel regions are

typically unknown, the profiles are determined from the experimental I-V characteristics in the sub-threshold by a reverse engineering process [5], [14] (see resulting values in Fig. 1). The 12 nm FinFET could be seen as a tri-gate version of the GAA NS FET that has a similar doping profile. The 12 nm gate length NW FET was scaled-down from a 22 nm gate length experimental transistor [15] previously studied in [14].

VENDES employs the finite-element (FE) method and combines 2D solutions of the Schrödinger (SCH) equation across the channel with the 3D drift-diffusion (DD) transport model and the 3D ensemble Monte Carlo (MC) technique in order to simulate the FETs in the sub-threshold and the on-regions, respectively [13]. The FE method allows to generate tetrahedral meshes that perfectly depict the real geometries as seen in Fig. 1. The 2D SCH equation quantum corrections incorporated into the 3D DD model permit a precise characterisation of the sub-threshold region. The 3D MC simulations consider all Si scattering mechanisms with Fermi-Dirac statistics in the screening of electron-ionised impurity scattering (self-consistently calculating Fermi level and electron temperature from electron density and average energy at the device mesh during each MC time step [16]).

This accurate modelling of electron transport in the highly doped source/drain regions assures a correct injection of carriers into the channel and reproduces correctly the experimental resistance in the source/drain [14], [17]. More details of the simulation procedures can be found in [13] whereas in-depth descriptions of the DD and MC physical models can be found in [18], [19].

To model the MGG, the gate work-function (WF) is modified using the Voronoi approach to represent the experimental shapes and values of the different grain orientations [20] (Fig. 1(e) lists the WF values and probabilities used for a TiN metal gate [21]). To introduce the LER, the edges of the device are deformed in the y-direction, which is perpendicular to the transport direction (see the reference axis in Fig. 1(d)). To generate the roughness profiles, Fourier synthesis with Gaussian auto-correlation [22] is used. The deformations are described by a root mean square (RMS) height that determines the amplitude of the roughness, and by a correlation length (CL) that accounts for the correlation in the transport direction between deformations (see the example in Fig. 1(e)). The GER follows a similar methodology to the LER, but the deformation profile is applied to the device gate (see the top example in Fig. 1(e)) [23]. To model the RDD in the n-type source/drain, a rejection technique is employed from the continuous doping of the ideal device (see the values in Fig. 1) [24], mapping the dopants to the tetrahedral mesh via the cloud-in-cell approach (see an example of the resulting electron concentration in Fig. 1(e)).

III. Comparison of Variability

All the study is done at a high drain bias, $V_{\rm DD}$=0.7 V. The threshold voltage ($V_{\rm T}$) is calculated using the constant current method [25] set to $I_{\rm D} = 2.0$ μA/μm. The on-current (I_{on}) is the drain current at $V_{\rm G}$= $V_{\rm DD}$+$V_{\rm T}$. To obtain statistical significance, ensembles of 300 devices are generated for each source of variability and for each analysed parameter.

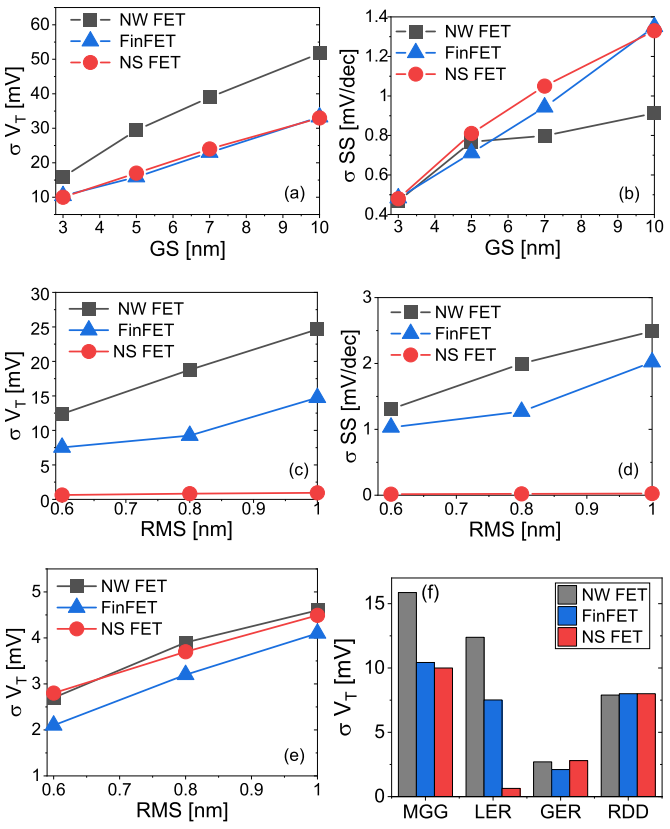

Figure 2. (a) Threshold voltage (σV_T) and (b) sub-threshold slope (σSS) standard deviations due to the MGG vs. the grain size, (c) σV_T and (d) σSS due to the LER vs. the root mean square (RMS) for a correlation length (CL) of 20 nm, (e) σV_T due to the GER vs. the RMS value (CL=20 nm), and (f) a comparison of σV_T vs. the source of variability for the three architectures (GS=3 nm and RMS=0.6 nm).

Figs. 2(a)-(b) show the $V_{\rm T}$ and SS standard deviations (σ) due to MGG as a function of the metal-gate grain size (GS), respectively, for the three analysed architectures. The NS FET and the FinFET exhibit less $V_{\rm T}$ variability than the NW architecture. We can observe that, the smaller the gate area ($G_{\rm A}$), the larger the expected variations. For instance, the σV_T for the NW FET ($G_{\rm A} \approx 395$ nm^2) is 59% larger for a GS=3 nm than those of the FinFET and the NS FET ($G_{\rm A} > 1000$ nm^2). The FinFET and NS FET exhibit an almost identical response to the $V_{\rm T}$ induced MGG variability with their σV_Ts linearly increasing with the GS. However, for the NW FET, σV_T begins to saturate at large GSs because of the very low number of grains present in the gate (≈ 4 grains when GS=10 nm) and the statistics follows a bimodal distribution. This saturation is even more noticeable in the σSS for the NW FET at GS equal or larger than 7 nm. However, the FinFET and the NS FET V_T and SS distributions are normal for all the analysed GS values.

Figs. 2(c)-(d) show, respectively, σV_T and σSS due to LER as a function of the RMS height for a CL of 20 nm. Previous SEM (Scanning Electron Microscope) studies [22], [26] showed CL values in the range of $20 - 80$ nm. The influence of LER on the NS FET is negligible, with σV_T values around 12 and 19 times lower than those of the FinFET and NW

FET, respectively (at RMS= 0.6 nm). LER is induced by resist patterning [27], and as previously mentioned, the LER deformation is applied in the y-direction, which corresponds with the critical dimensions for the FinFET (5.0 nm) and NW FET (7.5 nm). However, the critical dimension of the NS FET is its height (z-direction) that will not be affected by LER since is defined by epitaxial growth [6]. The width of the NS FET (50 nm) is large enough to remain practically unaffected by any LER deformation. Although the FinFET has a smaller width than that of NW FET, its larger height (50 nm) implies a larger conduction area, which reduces the potential impact of a LER deformation and explains the lower σV_T and σSS when compared to those of the NW FET. In addition, for the FinFET and NW FET, the LER induced σSS is generally larger than that observed for the MGG variability. Bear in mind that MGG, unlike LER, mainly implies a threshold voltage shift in the I-V characteristics.

Fig. 2(e) shows σV_T due to GER as a function of the RMS height for a CL of 20 nm. The influence of GER is significantly smaller than that of the other sources of variability analysed. Results show that the FinFET is less disturbed by the sub-threshold GER variability than the NS and the NW FET architectures. For example, at a RMS= 0.6 nm, the FinFET has a $\approx 20\%$ lower σV_T than those of the NS and the NW FETs (which are very similar). To understand the physical reason of this behaviour, for the FinFET and NS FETs we simulated configurations in which, keeping always the total device length fixed (40 nm), we increased/reduced L_{G} and therefore reduced/increased L_{SD} by 1 nm to account for the extreme deformation scenarios. We observed that a reduction/increase in L_{G} lead to a reduction/increase in the V_T value with respect to that of the 12 nm gate length device (δV_T). The FinFET and the NS FET presented the exact same δV_T values, which indicated a similar sensitivity of the two architectures to gate deformations. Therefore, the lower variability yielded by the FinFET can be explained due to the part of the gate located over the BOX regions (see schemes in Figs. 1(a) and (d)) which span over 10 nm. Any GER deformation falling in these zones will not affect the device behaviour, but will lower the statistical impact of the GER variability in the FinFET.

Fig. 2(f) shows the V_T variation for the four different sources of variability. For each source, the configurations that yield the lowest variability (i.e., a GS= 3 nm for MGG and a RMS= 0.6 nm for LER and GER) are selected. The three architectures have the same resilience (σV_T= 8 mV) to the RDD variations. Note that, as indicated in Fig. 1, they all have the same S/D length and N_{SD} doping. The RDD variations in the FinFET are larger than those previously reported for a similar gate length device [11], with a σV_T around 5 mV. Whereas in [11] they report rare extreme cases with a single dopant in the channel, in our devices the decay of the gaussian doping happens relatively close to the gate region, increasing the probability of finding one (or even more) dopants in this zone. If the exponential decay of the S/D doping were to happen 1 nm farther away from the gate, there is a 50% decrease in the observed σV_T due to RDD, highlighting the need for a nanoscale precision of ion implantation. In general,

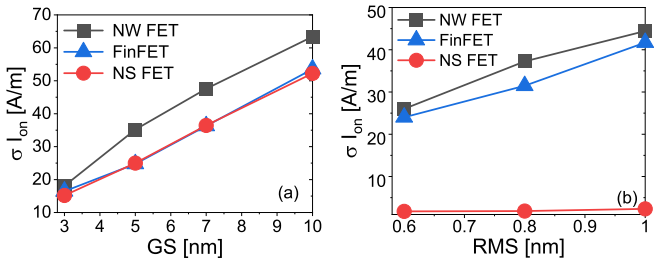

Figure 3. On-current standard deviation (σI_{on}) due to (a) the MGG and (b) the LER variability as a function of the GS and the RMS height, respectively.

the MGG and the LER are the two sources of variability that influence the device performance in the sub-threshold region the most. Therefore, the on-region study of variability is limited to these two sources since MC-based variability studies are very computationally demanding.

Figs. 3(a)-(b) show the I_{on} standard deviation due to MGG and LER, respectively. The I_{on} has been normalised by the semiconductor perimeter. Only the sidewalls and the top of the FinFET (see table included in Fig. 1) are considered to calculate this perimeter since the thick BOX at the bottom of the structure prevents any real effect in the device conduction. Similarly to what we observed for the sub-threshold region figures of merit, the NS FET and the FinFET are equally affected by the MGG variability in the on-region being more resilient architectures than the NW FET. At a GS= 3 nm, the NW FET σI_{on} is around a 20% larger than those of the NS FET and the FinFET. The LER induced variability also exhibits the same behaviour in the sub-threshold and on-region with a minimal influence of LER on σI_{on} in the NS FET (of around 2 A/m). The LER variability in the FinFET makes this architecture a slightly more resilient than the NW FET one. For instance, at a RMS=0.6 nm, σI_{on} due to the LER for the FinFET is 24 A/m, a value 10% lower than that of the NW FET.

IV. Conclusion

The simulation study demonstrated that MGG and LER are the two sources of variability that influence the performance of the three analysed architectures (FinFET, NS FET, and NW FET) the most. However, the impact of MGG and LER can be greatly mitigated if the fabrication process substantially reduces the RMS and the GS values. The NW FET is the least resilient architecture against these two sources of variability, specially in the sub-threshold region, with σV_T values at least 50% larger than those of the FinFET and the NS FET. The three architectures are equally affected by the RDD variability while the effect of the GER is very small. When compared to the FinFET, the NS FET is similarly affected by the MGG variations but the effect of the LER on the NS FET is negligible indicating that this architecture is a suitable candidate to replace FinFETs from a variability point of view.

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