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Laser Power Converter Architectures Based on 3C-SiC with Efficiencies >80%

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High power laser transmission technology is based on energy transfer through a monochromatic laser onto a photovoltaic receiver avoiding the limitations of conventional wiring. Current technology, headed by GaAs-based devices, faces two limitations: the intrinsic entropic losses and the degradation at high input power densities due to ohmic losses. Two novel laser power converters focused on overcoming these limitations are proposed. 3C-SiC is used as base material because of its high bandgap (2.36 eV) and its excellent crystallographic properties in order to reduce the entropic losses. Also, the current decreases due to the inherent flux reduction of high energy photons. To minimize ohmic losses, a recently proposed vertical architecture is explored, which can significantly reduce series resistance around two orders of magnitude ($\approx 10^{-5}\,\Omega\,cm^2$). Furthermore, 3C-SiC is also implemented in a conventional horizontal architecture to show the advantage of increasing the energy gap to reduce the ohmic losses. The two laser power converters obtain efficiencies above the state-of-the-art (87.4% at 3000 W cm^{-2} for the vertical architecture and 81.1% at 100 W cm^{-2} for the horizontal architecture) Taking this into account, the new devices open a new route for ultrahigh efficiency remote powered systems.

1. Introduction

High power laser transmission (HPLT) has been pointed as a key development in the emerging technology of wireless power transfer (WPT)[1] which has become an increasingly profitable market.[2] HPLT is based on the emission of monochromatic light to transfer energy to a remote photovoltaic device or laser power converter (LPC). In this sense, HPLT represents a paradigm shift with the possibility of transferring around a hundred watts of power density to several kilometers distance without using wires. The technology allows to overcome the limitations of conventional wiring because it provides electrical isolation and a reduction of electromagnetic interference and electrical noise.[3] Applications of this technology include, among others, dual transmission of power and data,[4,5] and optical powering of Internet-of-Things devices,[6] remote antennas,[7] aerial vehicles[8,9] and satellites.[10,11]

The LPC state-of-the-art is mostly based on III–V compounds, being GaAs the most used material.[12] Multiple studies have achieved efficiencies over 50% using GaAs-based LPCs.[13–25] In fact, the current experimental record set by Helmers et al.[21] has an efficiency of 68.9% under an input power density of 11.4 W cm^{-2} with a single GaAs cell. However, the efficiency of this device suffers from degradation with increasing input power density due to ohmic losses. This is a relevant constrain of current HPLT technology as it strongly limits the amount of power density to be transferred to the remote system. In order to overcome this limitation, Outes et al.[22] proposed a new architecture through numerical simulations, a GaAs-based vertical tunnel junction which achieves efficiencies of more than 76% at 3000 W cm^{-2}. The benefits of this architecture are no shadowing effects from the front metal grid and a very low series resistance ($\approx 10^{-5}\,\Omega\,cm^2$).

Although this vertical architecture may mitigate the efficiency degradation at high input power densities, the advancement of the current LPC technology is hindered by the properties of the base materials employed. There are several studies reporting that the maximum efficiency achievable for a material increases with its bandgap,[26,27] as high bandgap materials reduce the intrinsic entropic losses. This limits the improvement of devices based on Si (1.11 eV) and GaAs (1.43 eV). High bandgap materials have been recently pointed as the key to develop a new generation of ultraefficient LPCs.[28]

Among the wide bandgap semiconductors, silicon carbide (SiC) has been extensively researched and commercialized in

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the last two decades, mostly due to its application in power electronics.[29] SiC is found in several polytypes, being the hexagonal 4H and 6H the most employed so far.[30] Efforts are being made to obtain high-quality cubic 3C crystals because of the high electron mobility and isotropic properties,[31] and the fact that 3C can be grown on large commercially available Si wafers, notably reducing fabrication costs.[32] SiC has not been considered for solar PV applications due to its high energy gap and poor solar spectrum absorption.[33] However, this material becomes very interesting in the context of laser power converters due to the properties previously mentioned. Despite of this, to the date, it has not been investigated as an alternative to current LPC technologies and its actual potential remains unknown.

In this work, we study the feasibility of 3C-SiC as a base material for LPC for the first time. We employ two different architectures, a conventional horizontal laser power converter (hLPC) and a vertical laser power converter (vLPC), based on the structure proposed by Outes et al.[22]. We carried out a series of optimizations for both architectures under several input power densities (P_{in}) with the aim to enhance the LPC efficiencies. The simulation procedure is based on Silvaco Atlas,[34] a trustable and well-known TCAD tool, widely employed for accurate simulations of semiconductors performance. We have considered all the relevant phenomena in order to achieve reliable results and the material properties are taken from an exhaustive literature review based on experimental data. This work is intended to show the potential of this material to produce a new generation of low-cost and high-efficiency LPCs beyond current state-of-the-art technologies.

2. Devices and Simulation

In this section we present the two architectures considered, as well as the simulation framework applied in this work, which includes the TCAD software and the models being used.

2.1. Device Architectures

We investigate the feasibility of 3C-SiC as a promising material for LPC through two different architectures shown in **Figure 1**: hLPC and vLPC. The single unit structure of both LPCs consists of four layers with p+/p/n/n+ doping types. The third dimension (depth) does not affect the carrier transport and density, and it is set to 1 μm without loss of generality in order to save computational costs. The depth of the devices is only limited by fabrication issues and as some of 3C-SiC processes are very similar to those of the Si, these are well known and commonly industrialized. We apply total transmittance for the incident light in the illumination area, emulating the behavior of an antireflective coating.

In the hLPC the incident light is parallel to the current flow and perpendicular to the anode and cathode. In this architecture, there is a trade-off between the optical path and the carrier diffusion length, as the absorption and transport processes take place in the same direction. To avoid an excessively long device in which the minority carriers do not survive, a textured reflective layer is placed at the bottom of the structure. This layer increases the optical path, greatly enhancing light absorption and photon recycling.[35]

In the vLPC, the incident light is perpendicular to the current flow and parallel to the anode and cathode. This architecture shows a drastic reduction of series resistance and the absence of shadowing due to the metal grid.[36–38] Another interesting feature is the possibility to connect several devices via tunnel junctions to increase the illumination area.[36] This could be achieved by monolithically growing multiple subcells on the top of each other, as in standard multijunction concentrator solar cells. In this sense, the viability of stacking up to 30 p/n junctions has already been proven.[39,40] Another method to increase the illumination area is via the arrangement of a multisegment series connection.[41]

2.2. Simulation Framework

This work was carried out using Silvaco Atlas Software,[34] a TCAD simulator able to provide realistic and trustable results when modeling a wide variety of electronic devices, including photovoltaic solar cells. For instance, Michael et al.[42] applied it in the design and optimization of a III–V multijunction, Ochoa et al.[43] improved the efficiency of a multijunction

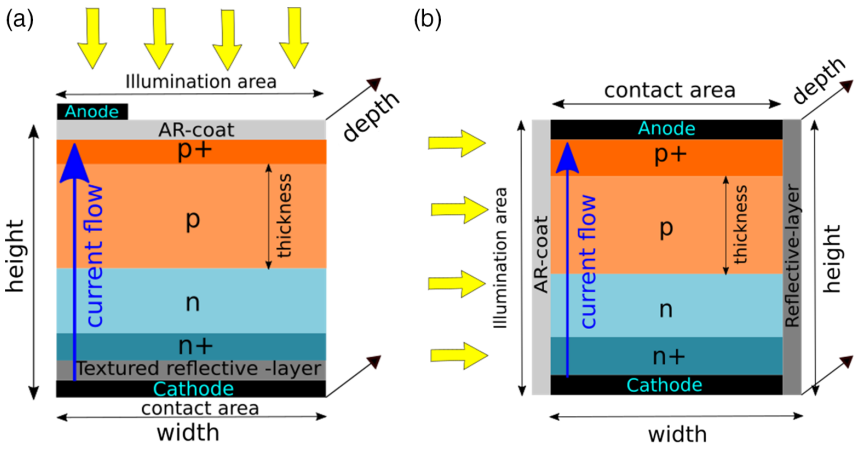

Figure 1. 2D single unit schemes of the a) hLPC and b) vLPC architectures. The third dimension of the two architectures (depth) is set to 1 μm. AR-coat is the antireflective coating.

concentrator under 5000 suns by optimizing the window layer and Seoane et al.[38] studied a vertical tunnel junction under 15 000 suns. ATLAS was also applied to design and optimize vertical laser power converters by Outes et al.,[22] and to evaluate the impact of design variables in a vertical epitaxial heterostructure architecture (VEHSA) LPC by York et al.[44]

In this work, Poisson and continuity equations were solved to obtain the main properties and characteristics of each device configuration. To realistically emulate the behavior of silicon carbide, we use the Caughey–Thomas model to describe carrier mobilities with doping density dependence,[45] a suitable model when a low electrical field is accounted.[46] Carrier mobility (μ) is expressed as

$$\mu = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + (N/N_{\text{ref}})^{\alpha}} \tag{1}$$

where $\mu_{\max}$ and $\mu_{\min}$ are the mobilities of pure and high doped crystal, respectively, N is the doping level, N_{ref} is the doping level at which the mobility is in an intermediate value between $\mu_{\min}$ and $\mu_{\max}$, and α is a fitting parameter. **Table 1** shows the mobility parameters used in this work.

We consider Shockley–Read–Hall (SRH) and Auger recombinations. After a preliminary study, we have found that the contribution of radiative recombination has no relevance because the radiative coefficient for 3C-SiC is an order of magnitude smaller than that of Si[48,49]; and therefore it has not been included in the simulations.

SRH recombination is considered the main recombination process in indirect bandgap semiconductors.[50] The SRH recombination rate ($R_{\text{net}}^{\text{SRH}}$) with doping dependence is expressed as follows

$$R_{\text{net}}^{\text{SRH}} = \frac{np - n_i^2}{\tau_p\left(n + n_i \exp\frac{E_{\text{trap}}}{k_B T_L}\right) + \tau_n\left(p + n_i \exp\frac{-E_{\text{trap}}}{k_B T_L}\right)} \tag{2}$$

where

$$\tau_{n,p} = \frac{\tau_0}{1 + \left(\frac{N}{N_{\text{norm}}}\right)^{\gamma}} \tag{3}$$

n and p are the electron and hole concentrations, n_i is the intrinsic carrier concentration, which is negligible for 3C-SiC at room temperature,[46] E_{trap} is the difference between the trap energy level and the intrinsic Fermi level, k_B is the Boltzmann constant, T_L is the lattice temperature, $\tau_{n,p}$ is the effective electrons and holes lifetimes, τ_0 is the longest lifetime observed in undoped crystal, N_{norm} is a doping concentration which operates as a normalization constant, and γ is a fitting parameter.[51,52] We use $E_{\text{trap}} = 0$, which corresponds to the most efficient recombination centers.[34] Although carrier lifetimes in SiC heavily depend on the crystal growth conditions, under low injection levels, lifetimes of up to 15 μs in 3C-SiC bulk are reported in the literature.[31] At low illumination levels, SRH dominates the recombinations because there are a large number of traps available. However, an increase in the input power density leads to higher SRH lifetimes due to a lower percentage of vacant traps compared to the excess carrier concentration.[53] To account for this effect, we increase the τ_0 lifetime with the excess carrier concentration following the trend observed in Hayashi et al.[54] We apply, for hole lifetimes, $\tau_p = \tau_n/5$, which is an usual relation in silicon and SiC.[55]

The Auger recombination rate (R_{Auger}) is determined by the following expression

$$R_{\text{Auger}} = C_n(pn^2 - nn_i^2) + C_p(np^2 - pn_i^2) \tag{4}$$

where C_n and C_p are the Auger experimental coefficients for a given material.[56] **Table 2** shows the set of recombination parameters used in this work. A remarkable characteristic of 3C-SiC is its small Auger coefficient, an order of magnitude less than that of Si and 4H-SiC,[57,58] and two orders of magnitude lower than in GaAs.[59] This is beneficial at high injection levels, when this recombination mechanism is predominant.[53]

In this study we consider bandgap narrowing with doping dependence and ideal surface passivation. All simulations were performed at a constant temperature of 298 K. The absorption coefficient with incident wavelength dependence is taken from experimental data.[60]

3. Results and Discussion

We initially present the optimization results for the hLPC and vLPC architectures under several P_{in} values and, at the end of the section, compare the efficiency of the proposed LPCs against that of several state-of-the-art devices. Optimization is performed by a multivariable iterative process, varying the parameters (layer thicknesses, doping concentrations, device width, incident wavelength) in discrete steps with the target of increasing the

Table 1. 3C-SiC mobility parameters for electrons and holes, extracted from refs. [32,47]. $\mu_{\max}$ and $\mu_{\min}$ are the mobilities of pure and high doped crystal respectively, N_{ref} is the doping level at which the mobility is in an intermediate value between $\mu_{\min}$ and $\mu_{\max}$, and α is a fitting parameter.

Mobility parameters			
Mobility model	Parameter	Electrons	Holes
Caughey–Thomas	$\mu_{\max}$ [cm^2 Vs^{-1}]	900	70
	$\mu_{\min}$ [cm^2 Vs^{-1}]	40	15
	N_{ref} [cm^{-3}]	1.5×10^{17}	5×10^{19}
	α	0.8	0.3

Table 2. 3C-SiC recombination parameters used during the simulations, extracted from refs. [31,55,58]. N_{norm} is a reference doping level which operates as a normalization constant, E_{trap} is the difference between the trap energy level and the intrinsic Fermi level, γ is a fitting parameter, and C is the Auger experimental coefficient.

Recombination parameters			
Recombination model	Parameter	Electrons	Holes
Shockley–Read–Hall	N_{norm} [cm^{-3}]	1×10^{17}	1×10^{17}
	γ	0.3	0.3
	E_{trap}	0	0
Auger	C	3×10^{-32}	2×10^{-32}

efficiency. The p+ and n+ layers are initially optimized, finding that their optimal values are a 40 nm thickness and 5×10^{19} cm^{-3} doping concentration for all the hLPC devices, and a 50 nm thickness and 8×10^{19} cm^{-3} doping concentration for all the vLPC devices studied. Next, we optimize the p and n layers thicknesses and doping concentrations. In the hLPC, we set the device width to 10 μm because no surface recombination is accounted in this work as first step, avoiding perimeter recombination sources, and the generation and transport processes occur in the vertical direction. However, in the vLPC, the width of the device needs to be considered. As the depth (the third dimension) does not affect the efficiency of these devices, both architectures can scale in that direction, increasing the illumination area and thus the incident power to the desired values as much as manufacturing processes allow it. The optimum incident wavelength is 525 nm for all the studied devices.

3.1. hLPC Optimization Results

Table 3 shows the optimum device structure and the main figures of merit that characterize the hLPC behavior, i.e., the short-circuit current (I_{SC}), the short-circuit current density (J_{SC}), the quantum efficiency (QE), the open-circuit voltage (V_{OC}), the voltage at the maximum power point (V_{MP}), the fill factor (FF), and the device efficiency (η). J_{SC} is obtained from dividing I_{SC} by the electrical contact area of the hLPC (the width of the device times the depth). For the lower P_{in} values ranging from 1 to 100 W cm^{-2}, the optimal layer thickness varies between 65 and 70 μm for the *p*-layer and is 9 μm for the n-layer. For 1000 and 3000 W cm^{-2}, the thickness is reduced to 49 and 40 μm, respectively, in the *p*-layer and to 6 μm in the *n*-layer. The optimum *p*-layer doping concentration increases with P_{in}, ranging from 5×10^{16} cm^{-3} at 1 W cm^{-2} to 1×10^{18} cm^{-3} at 3000 W cm^{-2}, while the n-layer doping concentration is 1×10^{14} cm^{-3} for all the P_{in} values studied.

Figure 2 shows the normalized *I–V* curves for the hLPC architecture. At P_{in} values ranging from 1 to 100 W cm^{-2}, the effect of the series resistance is not relevant, becoming noticeable at 1000 W cm^{-2} and significantly degrading the performance of the hLPC at higher P_{in} values.

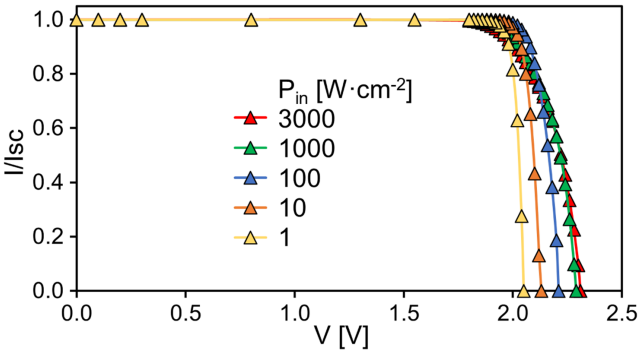

Figure 2. *I–V* curves, normalized to each I_{SC}, for various optimized input power densities (P_{in}) in the hLPC. The incident wavelength is 525 nm for all the P_{in} values.

QE is almost constant for the lower P_{in} values, slightly decreasing at 1000 and 3000 W cm^{-2} mainly due to Auger recombination. Also, although V_{OC} increases over the whole range of illumination, V_{MP} does not follow this trend, reaching a peak at 100 W cm^{-2} and then decreasing at higher P_{in} values. This can be mainly attributed to the series resistance, which produces a continuous decrease in FF from 92.7% at 1 W cm^{-2} to 80.3% at 3000 W cm^{-2}. The efficiency grows with the P_{in} from a 77.5% at 1 W cm^{-2} until it reaches a maximum of 81.1% at 100 W cm^{-2} and then, as a result of the increase of series resistance and Auger recombination, it decreases to 73.6% at 3000 W cm^{-2}.

3.2. vLPC Optimization Results

Table 4 shows the optimum device dimensions and main figures of merit. As the illumination area changes with the optimization processes, the total input power in the different vLPC structures may vary. The QE is a useful parameter in order to perform a fair comparison of these devices. Optimum *p*-layer remains at 51 μm

Table 3. hLPC optimization results and figures of merit for different input power densities (pin) values. The *p*- and *n*-layer thickness and doping concentrations are optimized. The I_{SC}, J_{SC}, QE, V_{OC}, V_{MP}, FF, and η are shown. The incident wavelength is 525 nm for all the pin values.

P_{in} [W cm^{-2}]		1		10		100		1000		3000	
Optimized structure	Layer	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]
	p	65	5×10^{16}	70	1×10^{17}	65	3×10^{17}	49	5×10^{17}	40	1×10^{18}
	n	9	1×10^{14}	9	1×10^{14}	9	1×10^{14}	6	1×10^{14}	6	1×10^{14}
	Width [μm]	10		10		10		10		10	
	J_{SC} [mA cm^{-2}]	4.08×10^{2}		4.10×10^{3}		4.10×10^{4}		4.06×10^{5}		1.19×10^{6}	
	QE	0.964		0.968		0.968		0.958		0.936	
	V_{OC} [V]	2.05		2.13		2.21		2.29		2.31	
	V_{MP} [V]	1.92		1.98		2.02		1.94		1.92	
	FF [%]	92.7		91.8		89.3		82.8		80.3	
	η [%]	77.5		80.0		81.1		76.9		73.6	

Table 4. vLPC optimization results and figures of merit for different input power densities (pin). The *p*- and n-layer thickness and doping concentrations are optimized, as well as the vLPC width (see Figure 1b)). The I_{SC}, J_{SC}, QE, V_{OC}, V_{MP}, FF, and η are shown. The incident wavelength is 525 nm for all the P_{in} values.

P_{in} [W [cm]$^{-2}$]		1		10		100		1000		3000	
Optimized structure	Layer	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]	Thick [μm]	Doping [cm^{-3}]
	p	51	5×10^{16}	51	5×10^{16}	42	3×10^{17}	27	5×10^{17}	18	5×10^{17}
	n	1	1×10^{17}	1	1×10^{17}	1	1×10^{16}	1	1×10^{16}	0.1	1×10^{16}
	Width [μm]	360		360		360		360		360	
	J_{SC} [mA cm^{-2}]	6.42×10^{1}		6.09×10^{2}		5.33×10^{3}		3.29×10^{4}		6.39×10^{4}	
	QE	0.988		0.994		0.992		0.994		0.995	
	V_{OC} [V]	2.04		2.10		2.16		2.21		2.23	
	V_{MP} [V]	1.92		1.98		2.04		2.08		2.10	
	FF [%]	93.2		93.2		93.3		93.0		92.9	
	η [%]	79.7		82.5		84.8		86.6		87.4	

for the two lower P_{in} values, and for 100, 1000, and 3000 W cm^{-2} is reduced by a 17.6%, 47.1%, and 64.7%, respectively. As the P_{in} increases, SRH recombination saturates, and Auger recombination mechanism becomes more relevant. Given that the thickness of the layers in the vertical architecture modifies the illumination area, the optimal thickness tends to shrink with increasing P_{in} in order to reduce the carrier concentration and thus Auger recombination. *N*-layer optimum thickness is 1 μm for all the P_{in} values except for 3000 W cm^{-2}, where it decreases to 0.1 μm. The optimum *p*-layer doping increases one order of magnitude over the entire P_{in} range, as the n-layer doping decreases by one order of magnitude. The total width of the device remains at 360 μm for all the P_{in} values studied. As in the vertical architecture there is no trade-off between photon absorption and carrier transport, the width of the device is independent of illumination and is adjusted for optimal absorption.

Figure 3 shows the vLPC normalized *I*–*V* curves for the P_{in} studied range. Note that for this architecture there is not any noticeable degradation due to series resistance at any P_{in} value, unlike in the hLPC. QE values are similar for all vLPCs, reflecting a steady internal conversion between incident photon-collected pair. V_{OC} and V_{MP} grow linearly with the logarithmic increase of P_{in}. FF is around 93% for all optimizations, indicating almost negligible series resistance losses. Efficiency grows linearly with the logarithmic increase of P_{in} for the studied range. This result, opposed to the behavior in the hLPC, comes from low series resistance and the lesser presence of Auger recombination in the vLPC architecture. Note that, the carrier density is lower in the vLPC architecture than in the hLPC because the absorption is made along the entire width of the device without photon recycling.

Comparing the two architectures, the QE is greater in the vLPC for all the P_{in} values studied, and no degradation appears in this parameter, in contrast to what happens in the hLPC. This is due to the regulation of incident light in the vLPC by the thickness of the layers, managing the excess carrier concentration and thus Auger recombination. **Figure 4** shows V_{OC} and V_{MP} for the hLPC and vLPC under several P_{in} values. For the two architectures, V_{MP} has similar values and grows linearly with the

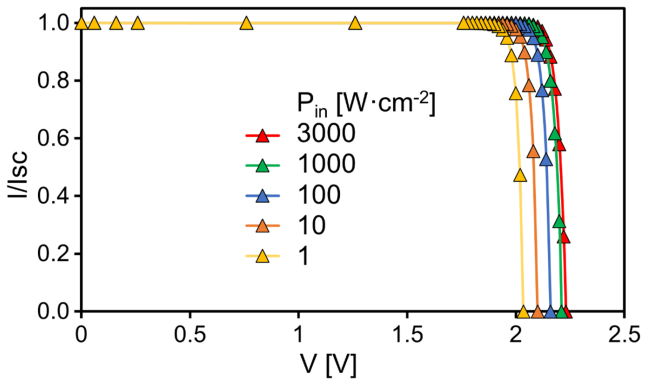

Figure 3. *I*–*V* curves, normalized to each I_{SC}, for the input power densities (P_{in}) optimized in the vLPC architecture. The incident wavelength is 525 nm for all the P_{in} values.

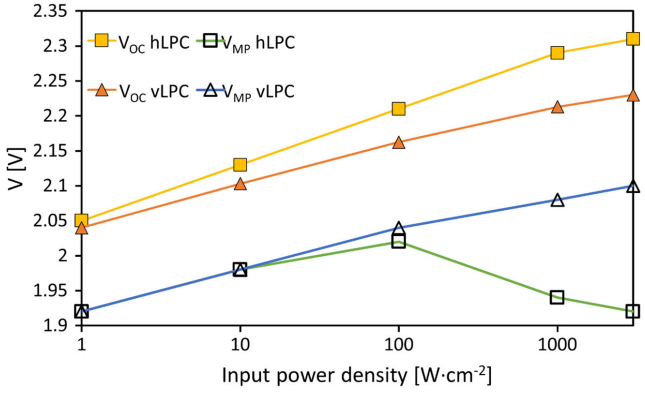

Figure 4. V_{OC} and V_{MP} dependence on input power density (P_{in}) for the hLPC and vLPC architectures. The incident wavelength is 525 nm for all cases.

logarithm of the P_{in} at low illumination rates. This progression continues in the vLPC for larger illumination rates, while in the hLPC a degradation of the FF and the V_{MP} appears at 100 W cm^{-2} and above due to series resistance. V_{OC} also grows linearly with the logarithm of the P_{in} in both architectures until Auger recombination affects this parameter at extreme P_{in} values above 1000 W cm^{-2}. However, the vLPC shows a lower dependence on this phenomenon, as already commented. Indeed, the increasing rate of the V_{OC} for the hLPC up to 1000 W cm^{-2} is around 8%, while it is only around 6% (2% lower) above this value. On the contrary, the vLPC shows an increasing rate up to this value of around 6%, while it is only reduced to 5% (1% lower) above this P_{in} value. This also contributes to increasing the efficiency of the vLPC converter with P_{in} in a larger amount. In any case, these results also indicate that Auger recombination is not expected to limit the development of 3C-SiC converters for HPLT applications.

As can be also seen in this figure, the V_{OC} values for the vLPC architecture are lower when compared to those of the hLPC. This can be explained considering the decrease in photogeneration rate across the device width. In the hLPC, there is a trade-off between light absorption and carrier diffusion length. Indeed, a textured back layer is required to increase the optical absorption without drastically increase the recombination losses. This leads to high carrier concentration and therefore to a higher V_{OC}. In the vLPC, there is no such trade-off, as the light absorption occurs in a perpendicular direction to the current flow. This produces better absorption by enlarging the width of the device without affecting the carrier diffusion (see Figure 1). Due to the large width of the vLPCs (360 μm), the photogeneration rate decreases by one order of magnitude through the device. The collected charge, and therefore the V_{OC}, diminishes as light goes deeper into the vLPC. As the anode and cathode cover the entire width of the device, the overall V_{OC} value will correspond to the voltage in the area with less illumination. Therefore, the width of the vLPC must reach a compromise between being large enough to ensure the absorption of most of the beam and maintaining sufficient excess carrier densities to avoid V_{OC} degradation in the least illuminated areas.

3.3. Comparative with State-of-the-Art LPCs

Figure 5 shows the efficiency as a function of P_{in} for the LPCs studied in this work and for several experimental and simulated state-of-the-art LPCs available in the literature. The values shown in the figure corresponding to this work are for the optimum structures at each P_{in}. The state-of-the-art LPCs shown here are GaAs or AlGaAs/GaAs based, which is the current standard technology. Helmers et al.[21] have achieved a remarkable efficiency of 68.9% at 11.4 W cm^{-2} with the implantation of an optical cavity that minimizes transmission and thermalization losses. This is the highest efficiency achieved by an experimental LPC, and the largest for P_{in} values below 100 W cm^{-2}. The performance of their horizontal LPC is degraded at higher irradiances than 11.4 W cm^{-2} due to ohmic losses, decreasing to 59.3% at 76.6 W cm^{-2}. In order to allow higher power to be transferred, other horizontal designs, such as the VEHSA architecture, presented by York et al.,[24] implement the strategy of stacking multiple thin photovoltaic semiconductor subcells on the top of each other to divide current, and therefore reduce the series resistance losses, achieving efficiencies of 66% at 64.6 W cm^{-2}.

From our proposed architectures, the 3C-SiC hLPC shows a remarkable efficiency between 10 and 100 W cm^{-2}, which could be considered the typical operating range of LPCs. This hLPC, optimized at 10 W cm^{-2}, achieves a 80.0% efficiency, improving

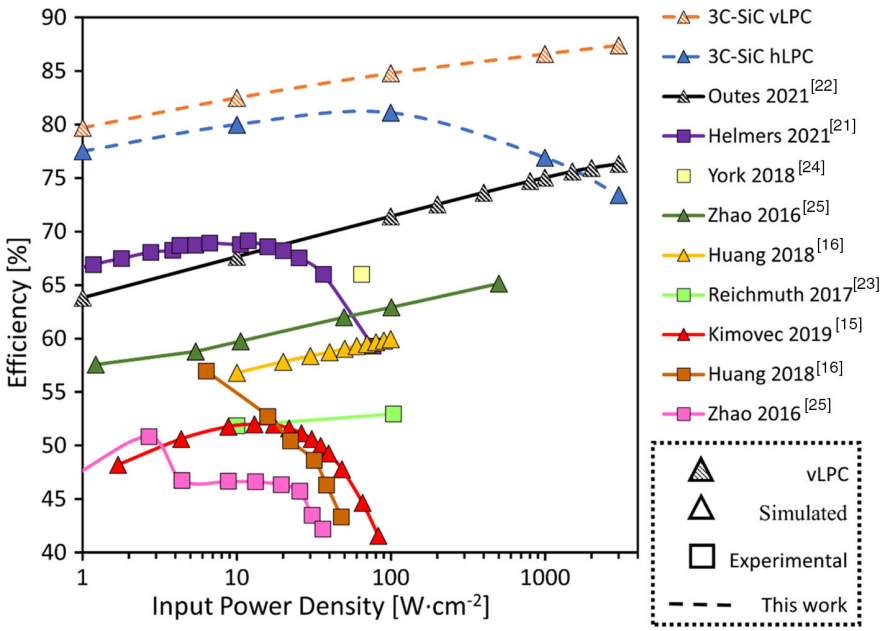

Figure 5. Efficiency versus input power density for present work and several state-of-the-art LPCs. vLPC and hLPC refer to the 3C-SiC architectures studied in this work. The LPCs shown correspond to Kimovec,[15] Huang,[16] Helmers[21] (illumination area of 0.054 cm^2), Outes,[22] Reichmuth,[23] York,[24] and Zhao.[25]

the current record of Helmers et al.[21] by 11.1%, and increases to 81.1% at 100 W cm^{-2}, exceeding by 9.7% the efficiency reported by the Outes et al.[22] simulated vLPC. At higher P_{in} values, like other horizontal LPCs, it suffers a decrease in efficiency due to growing series resistance losses and Auger recombination. However, the efficiency over all the analyzed P_{in} range is higher than that of the other state-of-the-art horizontal LPCs and the efficiency degradation is less abrupt, resulting in a 7.7% efficiency reduction from 100 to 3000 W cm^{-2}. Although the results above are expected to be lower for a real 3C-SiC hLPC device due to additional losses related to manufacturing constraints, e.g., shunt losses, surface recombination, etc., these results are promising to motivate further investigation on the development of highly efficiency novel LPCs based on 3C-SiC. Also, it is important to remark that the fabrication of 3C-SiC based devices is expected to be cheaper and more environmentally friendly than GaAs-based ones because it involves fewer toxic agents[61] and the fabrication processes have excellent compatibility with those used in Si, employing the same fab lines.

The 3C-SiC vLPC efficiency is higher than that of the 3C-SiC hLPC for all the P_{in} range studied, exceeding its efficiency in the typical operating range by a 2.5% at 10 W cm^{-2}, and by a 3.7% at 100 W cm^{-2}. At higher P_{in} values the vertical architecture does not appear to be limited by series resistance, as efficiency keeps growing linearly with the logarithm of P_{in}. The results of the 3C-SiC vLPC are also compared with those of the GaAs-based vLPC introduced by Outes et al.,[22] which established the previous efficiency record for a modeled LPC at high P_{in} values, achieving a 76.3% efficiency at 3000 W cm^{-2}. The 3C-SiC vLPC shows an extremely high efficiency of 87.4% at 3000 W cm^{-2}, increasing by 11.1% the result achieved by Outes et al. at this P_{in} value. This is noteworthy because the methodology used in Outes et al. is essentially the same than the one followed in his work. Hence, the difference in the results could mainly be attributed to the reduction of the current due to a lower photon flux density and more favorable materials properties of 3C-SiC compared to those of GaAs.

Possible limitations to this technology may arise from the manufacturing side, related to the illumination area. The device area of the state-of-the-art fabricated LPCs is 0.9 mm^2 for Reichmuth et al.,[23] around 3 mm^2 for Huang et al.[16] and Kimovec et al.,[15] 5.4 mm^2 for Helmers et al.,[21] and 11.3 mm^2 for Zhao et al.[25] In the hLPC architecture, the illumination area is defined by the width and depth of the device. As previously mentioned, we chose in this work a 1 μm depth for both architectures in order to save computational costs, and a 10 μm width in the hLPC single unit for the same reason. As the size of 3C-SiC wafers is around 200 mm,[62] the hLPC width and depth dimensions can be scaled up and consequently, the active area of this architecture can be in the order of cm^2 if needed. Hence, it would be possible to achieve the same areas than the state-of-the-art LPCs without manufacturing restrictions. In the case of the vLPC, the illumination area is determined by the depth and height of the device. As the depth can be scaled without performance degradation, the active area of a single vLPC unit, assuming a standard square geometry, is mainly limited by the optimum height, which is also going to depend on the incident power density. For instance, the total height is around 20 μm for an optimum vLPC unit at a P_{in} value of 3000 W cm^{-2}. This height could be small to achieve similar illumination areas to the state-of-the-art LPCs. However, this dimension can be increased through vertically stacking multiple tunnel junctions (VEHSA), as done in Fafard et al.[20] Indeed, it has been possible to vertically stack 30 units using tunnel junctions.[39] Taking this into account, the height of the vLPC device could be increased to around 0.6 mm. As commented, the depth can be scaled accordingly, achieving a total square 0.6 mm × 0.6 mm active area device, which is comparable to those of the state-of-the-art LPCs. These dimensions are also recommended because the goal of this architecture is to manage very high input power densities. Hence, an active area of less than 1 mm × 1 mm is recommended to reduce the heat waste and facilitate the thermal management.[63] Note that in the vLPC architecture the junctions are parallel to the light flow, and several identical single units can be vertically stacked without changing their structure, in order to obtain the same current in each single unit, so without increasing the series resistance losses.[22,38] This simplifies the design and makes it robust against temperature variations (due to change in energy gap and photon absorption), compared to the VEHSA architecture. Finally, it is important to mention that the active area of both architectures can be further increased if needed by arranging the single units onto a series/parallel-connected module.[15,64]

As previously commented, although the efficiency of 3C-SiC-based experimental LPCs could be reduced due to unexpected manufacturing issues, the simulation results indicate that this material opens a new promising route to improve the efficiency of current and future LPCs.

4. Conclusions

We have proposed cubic silicon carbide as base material for LPC because of its high bandgap and excellent crystalline properties. To study its suitability, we have considered two different architectures, a hLPC and a vLPC, whose design allows a reduction in series resistance. The devices are investigated by performing simulations with a TCAD software up to 3000 W cm^{-2}. In this work, the temperature is assumed to be constant and equal to 298 K, as the reference air temperature in the PV field. The increase of the temperature with the input power density and its effects on the device's performances are crucial for this technology to succeed, and many factors are involved (e.g., efficiency, area, thermal resistance, medium temperature, etc.).These effects were no considered at this stage of the investigation, although they will be carefully studied in future works.

Results show that, for both architectures, silicon carbide-based LPCs have better performance than GaAs-based LPCs in the whole illumination range studied. The 3C-SiC hLPC shows an efficiency of 81.1% at 100 W cm^{-2}, exceeding the current state-of-the-art record efficiency for hLPCs by 12.2%. Although at higher irradiances the performance of the 3C-SiC hLPC is degraded due to increasing series resistance and Auger recombination, the downgrading is less abrupt than in other hLPCs in the literature, indicating better performance at high injection levels.

The 3C-SiC vLPC improves the results of the state-of-the-art vLPCs by 11.1%, showing an efficiency of 87.4% at 3000 W.

The 3C-SiC vLPC shows no degradation over the entire power range studied, due to extremely low series resistance and a significantly reduced Auger recombination with respect to hLPC. As these mechanisms do not affect the device performance, the 3C-SiC vLPC exhibits a linear growth of efficiency with the logarithm of input power density, allowing room for improvement at higher powers.

Although the performance of real LPCs based on 3C-SiC can be affected by manufacturing issues, these results support that 3C-SiC could be a promising candidate to replace GaAs as the base material for high-efficiency LPCs for all input power range.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

3C-SiC, high power densities, laser power converters, vertical structures, wireless power transfer

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