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LIGHT MICRO-ENERGY HARVESTING IN STANDARD CMOS TECHNOLOGIES

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Light Micro-Energy Harvesting in Standard CMOS Technologies

Don Esteban Ferro Santiago

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Light Micro-Energy Harvesting in Standard CMOS Technologies

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A mi familia

A person who never made a mistake never tried anything new

Albert Einstein

If you think education is expensive, try ignorance

Derek Bok

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15 de noviembre de 2018

Resumen

Se estima que en los próximos años los dispositivos electrónicos integrados en objetos de uso diario interconectados a través de Internet, lo que se conoce como Internet de las cosas (Internet of Things, IoT), superarán al número de teléfonos móviles inteligentes o smartphones. Hoy en día la vida de las personas no se entendería sin todos esos dispositivos que generan una inmensa cantidad de información (Big Data) y que permiten a las personas ser conscientes de lo que sucede en su entorno y en el mundo en general. Además de los dispositivos IoT, los dispositivos tipo "wearable" también llegaron a la vida de las personas para facilitar su día a día, sensorizando e informando tanto del entorno como de variables corporales. Finalmente, los dispositivos implantables supusieron una revolución dado que permiten el tratamiento específico y la monitorización constante de variables fisiológicas sin necesidad de visitar un centro médico u hospital de forma regular.

Sin embargo, todos estos dispositivos que conviven con las personas día tras día imponen varios retos desde el punto de vista del diseño electrónico. Estos dispositivos requieren, en general, un tamaño o factor de forma muy pequeño, lo que lleva en ocasiones a dispositivos sin baterías o baterías muy pequeñas. Así mismo, también necesitan un bajo mantenimiento, lo que implica diseños de muy bajo consumo de potencia para aumentar la duración de las baterías. Para superar estos retos, la recolección de energía se ha convertido en una solución extendida y viable.

Existen múltiples fuentes de energía en el entorno. Algunos ejemplos son la luz, gradientes térmicos, vibraciones, señales de radio frecuencia, etc. La aplicación determinará la fuente de energía más adecuada. Sin embargo, la luz tiene una gran densidad de potencia, por lo que a priori es la fuente más atractiva siempre que esté disponible. Además, el transductor de esta fuente de energía puede ser integrado con el resto de electrónica en un mismo chip, consiguiendo factores de forma muy pequeños. Por lo tanto, el objetivo de este trabajo de

tesis es el diseño de un sistema de micro-recolección de energía solar en tecnología CMOS estándar para alimentar circuitos de muy bajo consumo de potencia. Las tecnologías CMOS estándar no requieren máscaras adicionales durante el proceso de fabricación del chip, lo que reduce los costes de fabricación.

La energía solar puede recolectarse para alimentar directamente la electrónica en el mismo chip. Sin embargo, en general, el voltaje generado por las células solares integradas, también conocidas como fotodiodos, es demasiado bajo, entre 0.2 V y 0.5 V dependiendo de la iluminación, por lo que se necesita elevar esta tensión a niveles más altos, adecuados para alimentar los circuitos integrados en el mismo chip. Una solución es conectar en serie varios fotodiodos para sumar sus voltajes, no obstante, esta solución implica una pérdida de eficiencia en tecnologías CMOS estándar. Otra solución es utilizar convertidores DC-DC para elevar la tensión generada por las células solares.

Los convertidores DC-DC pueden agruparse en dos grandes categorías: inductivos y capacitivos. Los primeros son atractivos dado su alta eficiencia energética, sin embargo, su uso no está muy extendido debido a la baja calidad de los inductores disponibles en las tecnologías CMOS estándar. Los convertidores DC-DC de tipo capacitivo con capacidades en conmutación, también conocidos como bombas de carga, son particularmente atractivos porque pueden integrarse completamente con un factor de forma relativamente bajo.

Las bombas de carga elevan la tensión de entrada transfiriendo paquetes de carga de la entrada a la salida a través de una cadena de N condensadores. En esta tesis doctoral la tensión de entrada del convertidor DC-DC será el panel solar. La salida del mismo será de tipo capacitivo para poder almacenar la máxima energía posible.

En circuitos integrados, la eficiencia del convertidor DC-DC se ve muy afectada por las capacidades parásitas asociadas a los condensadores de vuelo. Éstas dependen de la tecnología de fabricación utilizada. La eficiencia energética se puede mejorar significativamente implementando la técnica de reutilización de carga, la cual se introdujo en los años 90. Esta técnica consiste en reutilizar la carga de las capacidades parásitas inferiores que normalmente se desperdicia durante el funcionamiento normal del circuito, llevando a mayores ganancias en el convertidor y mejores eficiencias en carga o energía.

En los convertidores DC-DC con capacidades en conmutación se pueden distinguir dos límites de funcionamiento. En el caso de pérdidas resistivas insignificantes, es decir, cuando en cada fase del reloj se completa el proceso de transferencia de carga entre los condensadores de vuelo, el convertidor opera de acuerdo al límite de conmutación lento (Slow Switching Limit,

SSL). En el caso donde las pérdidas resistivas gobiernan el comportamiento del convertidor, es decir, cuando en cada fase del reloj una corriente constante fluye entre los condensadores de vuelo y, por tanto, el proceso de transferencia de carga es incompleto, el convertidor opera en el límite de conmutación rápido (Fast Switching Limit, FSL). La aplicación particular dictará el régimen de funcionamiento del convertidor DC-DC. En el ámbito de la micro-recolección de energía se necesita una frecuencia de conmutación lenta para evitar un consumo excesivo de potencia dinámica, lo que conduce al régimen SSL.

El uso de modelos resulta en tiempos de simulación sensiblemente inferiores a los de las herramientas CAD, facilitando el estudio y diseño de convertidores DC-DC. El tiempo de simulación depende de la topología del convertidor DC-DC y del tamaño de los condensadores, pero simulaciones que tardan horas o días con herramientas CAD se pueden realizar en varios segundos con simuladores basados en modelos.

Además, los convertidores DC-DC con capacidades en conmutación se pueden modelar desde un punto de vista estático o dinámico. Estudiando un convertidor en el estado estacionario, se extrae información sobre la ganancia, área o eficiencia. Sin embargo, un análisis dinámico resulta esencial en ciertas aplicaciones, tales como recolección de energía, donde la salida del convertidor es normalmente de tipo capacitiva y por lo tanto necesitamos estimar el tiempo de respuesta y la cantidad de carga que el transductor debe aportar. Además, los modelos estáticos y dinámicos deberían incluir la técnica de reutilización de carga.

En la literatura se pueden encontrar diferentes modelos que estudian las bombas de carga desde un punto de vista estático. También se pueden encontrar modelos dinámicos, pero o no tienen en cuenta las capacidades parásitas, o son demasiado complejos para incluir todos los fenómenos relacionados con los convertidores DC-DC de tipo capacitivo. Por otra parte, no se ha descrito en la literatura ningún modelo que incluya la técnica de reutilización de carga. Por lo tanto, observamos una falta de modelos simples y a la vez precisos que ayuden en el diseño de convertidores DC-DC con capacidades en conmutación, gracias a su menor tiempo de simulación.

Consecuentemente, en esta tesis hemos desarrollado un modelo simple, preciso y reproducible para el estudio dinámico de las bombas de carga de dos fases de reloj no solapadas incluyendo la técnica de reutilización de carga. El modelo proporciona los valores de tensión y carga en cada condensador de vuelo y en la salida para cada instante de tiempo tanto para cargas de tipo capacitivo como de tipo corriente. El modelo tiene en cuenta las capacidades parásitas superiores e inferiores de los condensadores de vuelo de las bombas de carga, lo

que lleva a una mejor precisión que los modelos descritos en la literatura. También hemos propuesto y demostrado que las capacidades parásitas de los interruptores pueden incluirse como parte de las capacidades parásitas superiores e inferiores de los condensadores de vuelo, mejorando la precisión del modelo cuando los condensadores de vuelo y las capacidades parásitas del interruptor son del mismo orden. Hemos extendido el modelo para incluir la técnica de reutilización de carga, que puede ser de interés en aplicaciones de baja potencia, como micro-recolección de energía, donde la eficiencia energética es un parámetro de diseño de gran importancia. Esta técnica presenta mejoras significativas tanto en ganancia como en eficiencia con respecto a las soluciones existentes. Hemos validado este modelo en el régimen SSL, donde se maximiza la eficiencia de conversión de las bombas de carga con capacidades parásitas. También hemos propuesto una metodología para diseñar el convertidor DC-DC fuera del régimen SSL, que consiste en calcular el límite del régimen SSL en un espacio de diseño determinado asumiendo cierta pérdida de precisión. Hemos validado el modelo a través de simulaciones a nivel de circuito y a través de resultados experimentales, y comparado con los principales modelos en la literatura, disminuyendo el tiempo de simulación y ofreciendo una mejor precisión. Aunque es un modelo general para el diseño de bombas de carga, hemos ilustrado todo lo anterior con el diseño de convertidores DC-DC en el ámbito de la micro-recolección de energía, mostrando el compromiso entre tiempo de subida y eficiencia en carga. Finalmente, hemos desarrollado un simulador web del modelo propuesto ahorrando hasta 10000 veces en tiempo de cálculo en comparación con conocidos simuladores a nivel de circuito.

Si seguimos profundizando en los modelos de convertidores DC-DC con capacidades en conmutación, hay algunas aplicaciones en las que se necesitan bombas de carga negativas o inversoras. Este tipo de convertidores cambia la polaridad de la tensión de entrada. Por ejemplo, en las memorias tipo flash se necesitan bombas de carga inversoras para generar tensiones negativas para su programación. En el campo de la micro-recolección de energía, los convertidores DC-DC inversores se utilizan para reducir la resistencia de conducción de los interruptores de carga en los transductores termoeléctricos, o para generar una tensión de alimentación positiva a partir de una tensión negativa generada por una célula solar integrada. Así pues, ante la falta de modelos simples y precisos de convertidores DC-DC con capacidades en conmutación de tipo inversor, en esta tesis hemos desarrollado un nuevo modelo dinámico para estudiar las bombas de carga inversoras controladas por dos señales de reloj no solapadas tomando como punto de partida el modelo anterior. Hemos validado el modelo tan-

to con simulaciones a nivel de circuito como con resultados experimentales, demostrando una elevada precisión. Finalmente, hemos propuesto el diseño de una bomba de carga inversora de tipo Dickson en el ámbito de la micro-recolección de energía usando tecnología CMOS estándar de 0.18 μm, mostrando el efecto de la implementación de la técnica de reutilización de carga.

El siguiente paso en el modelado de convertidores DC-DC con capacidades en conmutación para micro-recolección de energía es tener en cuenta el transductor. Para el caso particular de captación de energía solar, se pueden encontrar diferentes ejemplos en la literatura donde se utilizan fotodiodos y convertidores DC-DC para alimentar parcial o totalmente los circuitos integrados. En algunos ejemplos se utilizan células solares externas para recolectar energía. Otros ejemplos son chips de visión con capacidad de recolección de energía. En algunos casos se emplea el mismo fotodiodo para capturar la imagen y para captar energía, y en otros se usa uno para cada tarea dentro del mismo píxel, pero en todos los casos se implementan convertidores DC-DC con capacidades en conmutación para elevar la tensión del fotodiodo hasta la tensión de alimentación del chip. En todos estos ejemplos, el diseño de la bomba de carga se realiza con herramientas CAD, sin la ventaja que supondría usar modelos que incorporen los transductores de energía. Su inclusión en el flujo de diseño de convertidores DC-DC es crucial para tener una visión completa de los requisitos de consumo de energía de todo el sistema. Algunos modelos de este tipo se presentan en la literatura, pero estos modelos en general son incompletos. Por ejemplo, no tienen en cuenta las capacidades parásitas, o están restringidos a una topología de convertidor concreta. Por lo tanto, los efectos de la unión de un fotodiodo y una bomba de carga nunca han sido publicados anteriormente en la literatura.

Así, tomando como punto de partida el modelo de bombas de carga introducido anteriormente, en esta tesis hemos desarrollado un modelo preciso, sencillo y reproducible para el análisis transitorio del efecto conjunto del fotodiodo y la bomba de carga controlada por dos señales de reloj no solapadas en el régimen SSL. El modelo conjunto permite, por lo tanto, incluir la etapa de recolección de energía en el flujo de diseño de los convertidores DC-DC. Hemos asumido un modelo clásico para el fotodiodo cuya corriente fotogenerada se extrae de simulaciones a nivel de dispositivo realizadas con ATLAS (SILVACO). El modelo conjunto tiene en cuenta tanto las capacidades parásitas superiores como inferiores de los condensadores de vuelo de los convertidores DC-DC, lo que lleva a una mejor precisión que la de los modelos abordados en la literatura. Hemos validado el denominado modelo conjunto de transductor y convertidor DC-DC mediante simulaciones a nivel de circuito, obteniendo una alta

precisión y una velocidad de cálculo hasta 1700 veces superior a la de una herramienta CAD. El modelo conjunto muestra que la tensión generada por una célula solar integrada conectada a un convertidor DC-DC con capacidades en conmutación varía incluso con iluminación constante, lo que provoca un error en la estimación del tiempo que necesita el convertidor DC-DC para alcanzar la tensión de salida deseada. Este fenómeno sólo puede reproducirse a través del modelo conjunto. También hemos demostrado que la tensión máxima de salida alcanzada por un convertidor DC-DC en el régimen SSL cuando se utiliza una célula solar como transductor de energía depende de la frecuencia de conmutación del convertidor. Finalmente, hemos demostrado la aplicabilidad del modelo a través de la optimización del tiempo de subida y la eficiencia en carga de tres topologías comunes de convertidores, en concreto los convertidores de tipo Dickson, Fibonacci y exponencial, en el caso particular de fotodiodos o células solares en el mismo sustrato de silicio que la circuitería del convertidor DC-DC en tecnología CMOS estándar de 0.18 μm para dispositivos implantables. Hemos elegido una estructura p+ sobre NWell para el fotodiodo con un tamaño total de 1 mm^2.

Hemos utilizado todos estos modelos en el diseño de un sistema de micro-recolección de energía solar con célula solar y circuitería en el mismo sustrato de silicio. Un sistema de micro-recolección de energía consiste, en general, en un transductor y en una unidad de gestión de energía (Power Management Unit, PMU). Hasta este punto hemos introducido un modelo para estudiar el bloque principal de una PMU, el convertidor DC-DC con capacidades en conmutación, y el efecto de conectar un fotodiodo al convertidor. En los siguientes párrafos mostramos como hemos utilizado ese modelo para diseñar una bomba de carga que hemos integrado en una PMU, y como también hemos diseñado los otros bloques esenciales de la PMU. Como resultado, hemos fabricado y medido un chip prueba de concepto en tecnología CMOS estándar.

El enfoque clásico consiste en una célula solar sobre un chip CMOS que incluye la PMU. Sin embargo, integrar la célula solar y los circuitos CMOS en un mismo substrato de silicio permite conseguir un factor de forma muy pequeño y un coste reducido. Este enfoque, sin embargo, lleva a varios desafíos de diseño de la PMU. En primer lugar, la potencia generada por el fotodiodo puede ser tan baja como unos pocos nW para las células solares integradas, lo que dificulta el trabajo sin señales de control o mecanismos externos de puesta en marcha de la PMU. Otro desafío en el diseño de la PMU es manejar un amplio rango de potencia de entrada. Tomando como referencia una célula solar integrada de 1 mm^2, la potencia de entrada puede variar de unos pocos nW a varios μW para un rango de iluminación de 100 lx

a 100 klx. Esto exige una PMU eficiente con seguimiento del punto de máxima transferencia de potencia (Maximum Power Point Tracking, MPPT) que consuma solo unos pocos nW.

Se pueden distinguir dos formas principales de implementación del MPPT: lazo cerrado y lazo abierto. El primero implementa algoritmos como el "hill climbing", donde la impedancia de entrada de la PMU se ajusta paso a paso para alcanzar el punto óptimo en función de la salida de la PMU, que se mide de forma discontinua para reducir el consumo de energía a costa de una respuesta lenta a variaciones rápidas de la entrada. El segundo enfoque se basa en mediciones de corriente o tensión del fotodiodo sin tener en cuenta la salida de la PMU. Este enfoque es menos complejo que el anterior, reduciendo el consumo de energía a costa de una menor precisión en el MPPT. Un ejemplo de este método es el método de voltaje fraccional en circuito abierto (Fractional Open Circuit Voltage, FOCV), que consiste en medir la tensión generada por el fotodiodo en circuito abierto, ya sea desconectando el transductor de la PMU y reduciendo así la potencia de entrada de la PMU, o utilizando un transductor piloto, lo que da como resultado un mayor factor de forma, siempre con el objetivo de modificar la impedancia de entrada de la PMU para que coincida con la impedancia de salida del fotodiodo, obteniendo así la máxima transferencia de potencia.

En la literatura se han publicado algunos ejemplos de sistemas de micro-recolección de energía con una célula solar externa, lo que implica un aumento del tamaño del sistema. También se pueden encontrar algunos ejemplos que integran el fotodiodo y el resto de circuitería en el mismo substrato de silicio, pero no incluyen MPPT o necesitan alguna señal externa para arrancar. Por lo tanto, en el marco de este trabajo de tesis hemos propuesto una nueva arquitectura para mejorar las soluciones actuales. La arquitectura de este novedoso sistema de micro-recolección de energía consiste en una célula solar integrada de 1 mm^2 que alimenta una PMU para elevar la tensión generada por el fotodiodo a una tensión de salida superior a 1.1 V, adecuada para alimentar circuitos de bajo consumo de potencia. El chip se ha fabricado en tecnología CMOS estándar de 0.18 μm alcanzando un factor de forma de 1.575 mm^2, incluyendo la célula solar. Este enfoque puede ser de interés en aplicaciones tales como dispositivos implantables, donde se requieren pequeños dispositivos con bajo mantenimiento y la capacidad de manejar amplios rangos de potencia de entrada. La arquitectura incluye un fotodiodo p+ sobre P-Well en un NWell sobre substrato P de 1 mm^2 como la única fuente de energía del sistema. El fotodiodo se conecta directamente a la PMU sin ningún condensador de entrada para ahorrar área. La PMU consta de un oscilador auxiliar que acciona una bomba de carga auxiliar para generar la tensión de alimentación del circuito de control y de los

interruptores de la bomba de carga principal. El oscilador principal y el convertidor DC-DC principal están apagados durante el proceso de arranque para reducir el consumo de energía. El convertidor DC-DC auxiliar empieza a funcionar cuando la tensión generada por el fotodiodo es lo suficientemente alta como para encender el oscilador auxiliar y activar el proceso de arranque. Los resultados experimentales demuestran que la PMU arranca a partir de potencias producidas por el fotodiodo de 2.38 nW sin necesidad de ninguna señal externa. La tensión de salida del sistema es proporcionada por el convertidor DC-DC principal, que eleva la tensión generada por el fotodiodo a un nivel de tensión superior a 1.1 V durante la fase de funcionamiento normal de la PMU. Las señales de reloj que necesita la bomba de carga principal son proporcionadas por el oscilador principal. El bloque MPPT ajusta la impedancia de entrada de la PMU para alcanzar una eficiencia máxima del 57 % durante el funcionamiento normal.

El bloque MPPT funciona en lazo abierto, continuo y en régimen bidimensional, es decir, modificando la frecuencia de las señales de reloj de ambas bombas de carga y tanto la ganancia como la capacidad por etapa de la bomba de carga principal, todo ello para manejar un rango de potencia de entrada de nW a μW. El bloque MPPT está siempre conectado al fotodiodo para determinar las diferentes zonas de trabajo en función de la iluminación. En otras palabras, el voltaje generado por el fotodiodo define las regiones de trabajo. En la fase de diseño hemos definido cinco regiones de trabajo diferentes mediante simulación para que el MPPT cubra el rango de tensiones de entrada del fotodiodo, por lo que hemos diseñado cuatro detectores de nivel para distinguir entre las cinco regiones de trabajo. Los detectores de nivel tienen una salida digital que es alta cuando la tensión generada por el fotodiodo es superior a la tensión de disparo del detector de nivel. Por lo tanto, este método de MPPT puede ser visto como una tabla de consulta (lookup table) definida en la fase de diseño. Esta aproximación de MPPT implica un consumo de potencia tan bajo que permite al sistema arrancar de potencias de entrada de nW, mejorando las soluciones propuestas en la literatura. Por último, una corriente de referencia autoajustable por medio de la tensión generada por el fotodiodo fija la frecuencia del oscilador auxiliar y también realiza un ajuste fino de la frecuencia del oscilador principal independientemente de la región de trabajo y, por tanto, de la topología de la bomba de carga.

Finalmente, el sistema de micro-recolección de energía introducido en los párrafos anteriores se ha presentado como una demostración en vivo en el 2018 International Symposium on Circuits and Systems (ISCAS). El sistema se iluminó con una lámpara para generar energía eléctrica y alimentar una puerta lógica externa situada en una placa de pruebas, mostrando las

señales de control y alimentación en un osciloscopio. Se demostró así el funcionamiento del sistema de micro-recolección de energía.

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Chapter 1

Introduction

Nowadays electronics has come into people's daily lives to improve their quality of life. Internet of Things (IoT) [1], wearable computing [2, 3] or implantable devices [4–6], are examples of applications without which people's lives could not be understood today. Nevertheless, from the point of view of electronic design, this presents some challenges such as achieving small form factor systems, high battery life or even batteryless systems. Several solutions like low-power design are implemented to overcome the above challenges. Besides, energy harvesting has become an extended and viable solution [4,5]. Energy harvesting allows to reduce the maintenance and increase the lifetime of the systems.

Some ambient energy source examples are light, thermal gradients, vibrations, RF radiation, and so on, being the light very attractive due to its great power density [7]. In addition, solar micro-energy harvesting allows to integrate sensing, processing and harvesting on the same silicon substrate resulting in significant area, power and cost savings [8].

Solar energy can be harvested to directly supply the integrated circuit [5,9]. Nevertheless, in general, the generated voltage is too low to power the electronics within the chip. A micro-solar cell or photodiode generates between 0.2 V and 0.5 V depending on the illumination [10]. A direct solution can be to stack photodiodes in order to obtain a higher voltage. However, this solution implies a decrease in the energy efficiency for standard CMOS technologies [11]. Other solution to address this problem is to use a voltage step-up converter such as a DC-DC converter. The DC-DC converters can be grouped in two main categories: inductive and capacitive DC-DC converters. The former are attractive because of their high efficiency [12–14], however, they are not widely used because of the poor quality of integrated inductors

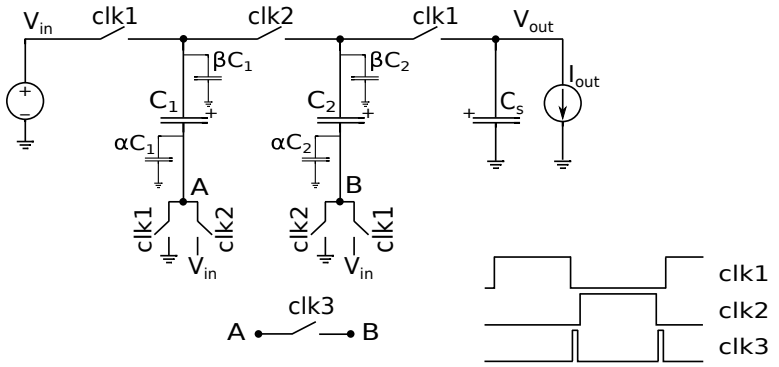

Figure 1.1: Schematic of a 2-stage Dickson charge pump (LQP3×) with clock signals *clk1* and *clk2*. The third clock signal, *clk3*, is used in the charge reusing approach. αC_j and βC_j are the bottom and top parasitic capacitances, respectively.

in standard CMOS technologies [15]. The latter, also called charge pumps, are particularly attractive because they can be fully integrated with a relative small form factor [8, 16–18].

Therefore, the final goal of this thesis is to design an energy harvesting system including a charge pump and the circuitry needed to manage the power generated by the on-chip solar cell in standard CMOS technology in order to power other circuits with low power consumption.

1.1. Capacitive DC-DC Converters

Charge pumps rise up the input voltage transferring charge packets form the input to a load through a chain of N capacitors. Dickson, also called linear charge pump (LQP) [19], Fibonacci (FQP) [20], or exponential (EQP) [21] are examples of classic capacitive DC-DC converters. As an example, Figure 1.1 shows a Dickson charge pump of 2 stages with 3× gain (LQP3×) and the clock signals needed for its operation. Also, other topologies derived from the classical ones can be found in [22–24].

On integrated circuits, the charge pump efficiency can be severely affected by the parasitic capacitances associated with the flying capacitors, which depend on the manufacturing technology. In Figure 1.1 such parasitic capacitances are shown for an LQP3× as αC_j and βC_j. Some typical values are 10% and 5% of the flying capacitor values for bottom and top parasitic capacitances, respectively [25, 26]. The charge pumps efficiency can be improved implementing the charge reusing technique, which was introduced in the 90s [27, 28]. It

consists of reusing the charge of the bottom parasitic capacitances which is normally wasted during the circuit operation, leading to higher gain and better charge or energy efficiency of the charge pump. This technique is applied to charge pumps in [29, 30], reaching significant improvements.

Regarding the charge pump operation, two limits can be distinguished. In the case where the resistive losses are negligible, i.e. the transferring process is completed during each clock phase, the converter operates according to the Slow Switching Limit (SSL). In the case where the resistive losses govern the charge pump behavior, i.e. a constant current flows between capacitors and therefore the transferring process is incomplete during each clock phase, the converter operates in the Fast Switching Limit (FSL). The particular application will dictate the operation regime of the charge pump. In micro-energy harvesting applications, charge pumps with low switching frequencies are the most appropriate in order to reduce excessive dynamic power consumption. Therefore, the charge pumps should operate in the SSL [31].

1.1.1. Charge Pump Models

Different models to study the performance of the DC-DC converters have been reported in the literature. Models are preferable to circuit simulations with Computer-Aided Design (CAD) tools because of their shorter computation time. The simulation time depends on both topology and capacitor values, but simulations which take hours or days with CAD tools can be performed in several minutes with model-based simulators.

Charge pump circuits can be studied in two different regimes, steady-state and transient-state. In the steady-state regime, information about gain, area or efficiency can be extracted [25, 32–41]. However, a dynamic analysis is essential in certain applications such as energy harvesting, where the load of the charge pump circuit is usually a capacitor being continuously charged and discharged according to the charge demanded by the system. In [42–45] the transient state of the LQP architecture is studied. A more general model for any charge pump in the SSL regime is introduced in [46], but the effect of parasitic capacitances is not illustrated. The model is then modified to include in FSL the effect of the switches' resistances which are supposed to be constant, resulting in inaccuracies. A circuit model described with average equivalent circuits is developed in [47, 48] and even though the model is very complete, additional steps are needed to obtain the average equivalent circuit model which represents the dynamic behavior, making the automation for complex topologies harder. Also, parasitic capacitances, which are significant in integrated circuits, are not included in the av-

erage circuit model. In [49] both steady-state and transient behavior of switched-capacitor DC-DC converters (SCC) are described by systems of linear equations, applying KVL and the charge conservation law. In [49] all the parasitic resistances of a real implementation are modeled by an equivalent resistance, whose value is calculated in a straightforward manner in SCC topologies where all capacitors are connected in series. Nevertheless, this is not a direct step for more complex topologies or circuits with parasitic capacitances. In [50] the SCC topologies are modeled through first-order differential equations and applying the charge conservation law, the voltage through all capacitors can be calculated in the SSL regime. In this paper, the authors also introduce a new average loss-based model based on [36], where the conduction losses are modeled by an equivalent resistance. As stated by their authors, the main disadvantages of this model are its very high nonlinear structure and that the accurate estimation of the equivalent resistance may not be an easy task. The model does not include parasitic capacitances either. Finally, the dynamic model addressed in [51] includes all parasitic capacitances but, as stated by their authors, it is very complex. The reason is that it covers the whole frequency spectrum from SSL to FSL. The complexity of this model makes it hard to reproduce it, as numerical simulations are needed. This model can be reduced to a first-order model, but to do this, the model must be converted to a discrete-time model, which may not be a direct step. Also, through the first-order model it is not possible to have information about the internal dynamics of the converter.

On the other hand, a solution to improve both efficiency and gain of charge pump circuits was reported in [29, 30]. It consists of charge reusing by adding a clock signal and some switches linking the bottom parasitic capacitances of the charge pumps. To the best of our knowledge, a model that reproduces the dynamic behavior of charge pumps implementing the charge reusing technique has never been previously reported in the literature.

So after considering all the models and methods which have been introduced above, we find a lack of simple and accurate models that help in the charge pump design process. Therefore, we have developed a reliable, simple and reproducible model for the transient analysis of two-phase charge pumps including the charge reusing approach [52]. The model provides both charge and voltage time responses at every flying capacitor and at the output for both current and capacitive loads. Our model was validated through circuit-level simulations and experimental results and compared with the main models in the literature, decreasing the simulation time and featuring better accuracy.

The main contributions of this thesis to the field of charge pumps modeling are reported

in [52] and reproduced in Chapter 2, and can be summarized as:

1. Our model accounts for both top and bottom flying parasitic capacitances of DC-DC converters. Also, we have proposed and demonstrated that parasitic capacitances from the switches can be included as part of the top and bottom parasitic capacitances, improving the accuracy of the model when the flying capacitors and the switch parasitic capacitances are of the same order.

2. The model was extended to the charge reusing or recycling technique, which might be of interest in low power applications, where the energy efficiency is a design parameter of utter importance, like in micro-energy harvesting, Dynamic Voltage Scaling (DVS), or Near-Threshold Voltage (NTV) logic. This technique features significant improvements in both gain and efficiency with respect to existing solutions.

3. The model is intended for the SSL regime, where the conversion efficiency of charge pumps with parasitic capacitances is maximized [31]. For this reason, an expression for the determination of the SSL boundary layer was derived. However, a methodology to design the DC-DC converter outside the SSL regime was proposed consisting of finding the SSL boundary layer in a given design space with a given error level when compared to the results from a circuit-level simulator. We have illustrated this methodology for the switching frequency-switching transistor width parameter space.

4. Although it is a general model for the design of charge pumps, we have illustrated all the above with the design of DC-DC converters for micro-energy harvesting constraints, showing the trade-off between time response and charge efficiency.

5. A web simulator of the proposed model was developed saving up to 10000× in computation time when compared to well-known circuit-level simulators [53].

More details about this model and how it helps in the design procedure of charge pumps can be found in Chapter 2.

If we continue delving into capacitive DC-DC converters models, there are some applications where inverting or negative charge pumps are needed. This kind of converters change the polarity of the input voltage. As an example, Figure 1.2 shows a 2-stage inverting Dickson charge pump with -2× gain (LQP-2×). For example, in several flash memories devices inverting charge pumps are needed in order to generate both positive and negative voltages

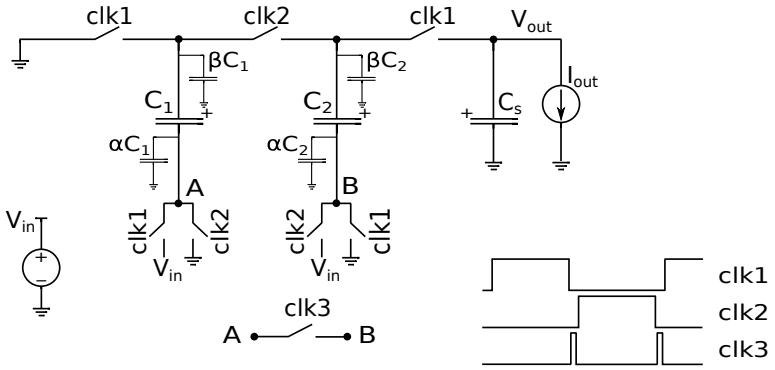

Figure 1.2: Schematic of a 2-stage inverting Dickson charge pump (LQP-2×) with clock signals *clk1* and *clk2*. The third clock signal, *clk3*, is used in the charge reusing approach. αC_j and βC_j are the bottom and top parasitic capacitances, respectively.

for programming the flash memory cells [24, 54]. In the energy harvesting field, inverting converters are used to reduce the on-resistance of load switches in thermoelectric harvesters [55], or to generate a positive supply voltage from a low negative voltage generated by an integrated micro-photovoltaic DC transducer [56, 57].

Noticing the lack of simple and accurate models shown above and extending the model presented in Chapter 2, we have presented a dynamic model for on-chip inverting charge pumps driven by two non-overlapping clock signals [58]. The model accounts for parasitic capacitances and was extended to account for the charge reusing technique. The model was validated through both circuit-level simulations and experimental results, demonstrating high accuracy. Finally, the design procedure of an inverting Dickson charge pump for micro-energy harvesting in standard 0.18 μm CMOS technology showing the effect of implementing the charge reusing technique was introduced. More details about the inverting capacitive DC-DC converter model implementing the charge reusing technique can be found in Chapter 3.

1.1.2. Joint Model of Harvester and DC-DC Converters

As we have introduced at the beginning of this Chapter, solar energy harvesting is very attractive in different applications as it allows to fabricate devices with very small batteries or even batteryless, reducing the maintenance and increasing their lifetime. Furthermore, in the case of integrated solutions, the photodiode used to recollect energy from light is fabricated in the same substrate as the sensing and processing core, decreasing the form factor and costs

[8]. As also explained at the beginning of this Chapter, DC-DC converters are needed to rise up the voltage generated by the photodiodes to useful levels to power other electronics within the chip, being capacitive DC-DC converters suitable for this task because they can be fully integrated. A simple, accurate and general model to help in the design of charge pumps overcoming the state-of-the-art has been also presented.

For the particular case of solar energy harvesting, different examples can be found in the literature where photodiodes and DC-DC converters are used to supply the integrated circuits partially or totally. For instance, in [4] a chip is designed to measure the intraocular pressure including a micro-solar cell and a DC-DC converter to supply a microcontroller. In [16, 59] the authors design a fully integrated energy harvester from a solar cell of 0.84 mm^2, and the generated voltage is raised up with a self-oscillating DC-DC converter. In [60–66] different vision chips which include solar energy capabilities are designed. In some cases, the same photodiode is used to capture the image and to harvest energy and, in other cases, different photodiodes are used for each task inside the pixel, but in all cases a DC-DC converter is necessary to rise up the generated voltage to the supply voltage. Also, in [56] an inductive DC-DC converter is implemented but, as explained, inductors can not be integrated with high quality in standard CMOS technologies.

In all the previous examples, the design of the charge pump is performed using CAD tools without micro-energy transducer models. However, their inclusion into the design flow of integrated circuits is crucial to have a complete view of the power consumption requirements of the whole system. In [22] authors propose a new DC-DC converter architecture for solar micro-energy harvesting based on LQP. The study of the converter is limited to the steady-state and the dynamics of the photodiode are not fully taken into account. In [12, 67] the DC-DC converters are analyzed from a theoretical point of view considering the photodiode designed for each case, but the DC-DC converter is inductive. In [10] authors show aspects of modeling and designing of the photovoltaic power conversion on chip, but the work is limited to the LQP charge pump and the charge consumed by the DC-DC converter itself is not taken into account. Finally, in [26] a new model to maximize the output power in systems with both DC energy transducer and DC-DC converter is proposed but it is restricted to the LQP in the steady-state.

Therefore, to the best of our knowledge, a general model that reproduces the dynamics of the joint effects of the photodiode and the charge pump has never been previously reported in the literature. So, taking as a starting point the model in Chapter 2, we have developed

an accurate, simple and reproducible model for the transient analysis of the joint effects of the photodiode and the charge pump driven by two clock signals [68]. We have assumed a classical model for the photodiode whose photogenerated current was extracted from device-level simulations with ATLAS from SILVACO.

The main contributions of this thesis in the field of joint modeling of charge pumps and transducers are conveyed in [68] and reproduced in Chapter 4, and can be condensed as:

1. Our model accounts for both top and bottom flying parasitic capacitances of DC-DC converters, which leads to better accuracy than the models reported in the literature.

2. The joint model was verified by circuit-level simulations achieving high accuracy and computation time savings of up to 1700×.

3. The joint model shows that the voltage generated by an integrated photovoltaic cell connected to a capacitive DC-DC converter is not constant even under constant illumination, leading to an error in the estimation of the time needed by the DC-DC converter to reach a given output voltage. This phenomenon can only be reproduced through the joint model.

4. We have also demonstrated that the maximum output voltage reached by a DC-DC converter in the slow-switching limit regime when a photovoltaic cell is used as energy transducer depends on the switching frequency.

5. The joint model is useful in the design process of capacitive DC-DC converters in the SSL region as it allows to include micro-energy harvesting stages into the design flow of the integrated circuits. The applicability of the model was illustrated through the optimization of time response and charge efficiency for LQP, FQP and EQP in the case of implantable devices for a target technology of 0.18 μm standard CMOS. The harvester was chosen to be a p^+ over P-Well in NWell photodiode with a size of 1 mm^2. To illustrate this topology, Figure 1.3 shows the on-chip photodiode connected to a Dickson charge pump with 3× gain.

More details about the joint model can be found in Chapter 4.

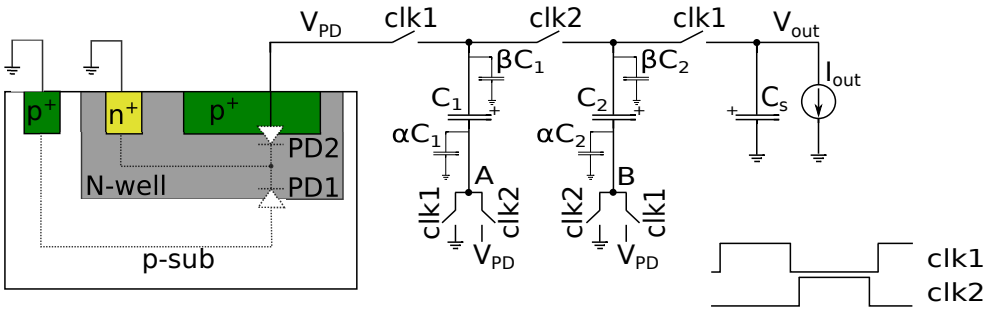

Figure 1.3: Schematic of a 2-stage Dickson charge pump (LQP3×) with an on-chip solar cell as harvester. *clk1* and *clk2* are the clock signals. αC_j and βC_j are the bottom and top parasitic capacitances, respectively.

1.2. Micro-Energy Harvesting System

A micro-energy harvesting system, in general, consists of a harvester and a Power Management Unit (PMU). In previous subsections, we have introduced a model to study the main block of a PMU, the capacitive DC-DC converter, and the effect of connecting the harvester to the converter. Next, we show how we have used that model to design a charge pump that we have integrated in a PMU, and how we have also designed the other essential blocks of the PMU.

The classical approach of light energy harvesting includes an off-chip solar cell stuck over a CMOS chip with a PMU [4]. Nevertheless, as we have seen at the beginning of this Chapter, by integrating the solar cell and the CMOS circuitry on the same silicon substrate, a very small form factor and reduced cost can be met [8]. This approach, however, leads to several design challenges of the PMU.

First, the scavenged power can be as low as a few nW for on-chip solar cells, making it hard to work with such low power levels without external control signals or start-up mechanisms [8,69]. Another design challenge is to handle a large input power range [13,18]. Taking as a reference an on-chip solar cell of 1 mm^2, the input power can vary from a few nW to several µW for an illumination range from 100 lx to 100 klx [10]. This demands an efficient PMU with Maximum Power Point Tracking (MPPT) consuming only a few nW. The works in [16,70,71] are examples of PMUs which do not include neither the transducer on the same substrate nor MPPT capability, making it difficult to manage such a large input power range. Conversely, in [8] a system which includes a transducer and a PMU on the same substrate is

presented, however, it does not include the MPPT capability.

Two main conventional ways to perform the MPPT can be distinguished: closed-loop and open-loop [72]. The first one implements algorithms such as hill climbing where the PMU input impedance is adjusted step by step to reach the optimal point depending on the PMU output, which is measured discontinuously to reduce power consumption at the cost of a slow response to rapid input variations [17, 73–75]. The second approach is based on current or voltage measurements of the photodiode without taking into account the PMU output. This approach is less complex than the former, reducing the power consumption at the cost of less accuracy in the MPPT. Some examples of the open-loop approach are the algorithm proposed in [76] and the fractional open circuit voltage method (FOCV) [18, 77]. The latter consists of measuring the open circuit harvested voltage either by disconnecting the main transducer from the PMU and thus decreasing the PMU input power, or by using a pilot transducer, resulting in a larger form factor, with the goal of modifying the PMU input impedance to match photodiode and PMU impedances.

As we have presented above, the design of a micro-energy harvesting system presents several challenges and limitations, therefore, we have proposed a new architecture to improve the current solutions. The architecture of this micro-energy harvesting system consists of a PMU powered by a 1 mm^2 on-chip solar cell to rise up the harvested voltage to an output voltage higher than 1.1 V, suitable for powering low-power circuits [78]. The PMU includes an MPPT block which performs an open-loop and continuous MPPT without disconnecting the photodiode from the PMU, overcoming the above mentioned limitations. The chip was fabricated in 0.18 μm CMOS technology. Our approach can be of interest for applications such as implantable devices, which demand long-time maintenance cycles along with the capability of handling low and wide input power ranges.

Figure 1.4 shows the proposed architecture. It includes a P^+ over P-well in N-well over P-substrate photodiode of 1 mm^2 as the only power source of the system. The photodiode is connected directly to the PMU without an input capacitor in order to save area. The PMU comprises an auxiliary oscillator driving an auxiliary charge pump to generate the voltage of the control circuit and the main charge pump switches. The main oscillator and DC-DC converter are OFF during the start-up process by means of power-gating to decrease energy consumption. The auxiliary DC-DC converter starts working when the voltage generated by the photodiode, V_{PD}, is high enough to switch on the auxiliary oscillator and to trigger the start-up process. The output voltage of the system, V_{out}, is provided by the main DC-DC

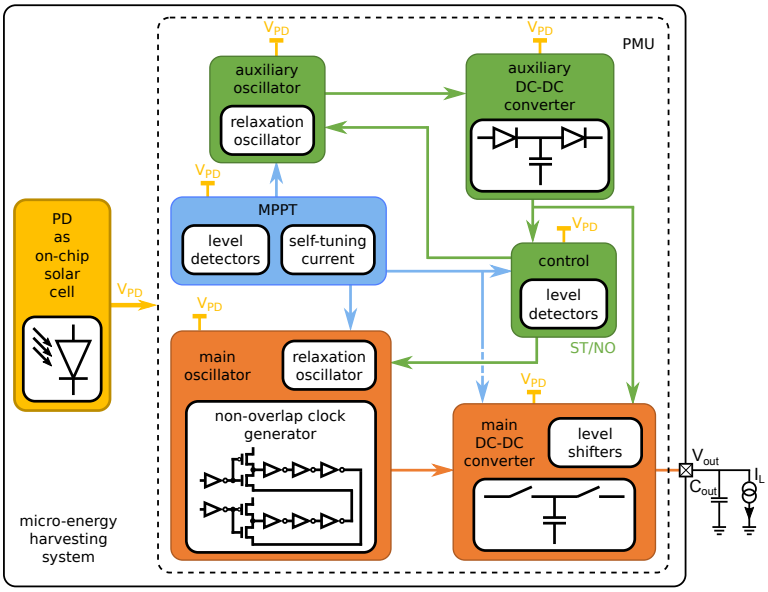

Figure 1.4: Architecture of the proposed micro-energy harvesting chip which includes an on-chip solar cell and a PMU on the same substrate.

converter, which rises up the voltage generated by the photodiode to a voltage level above 1.1 V during the normal operation phase of the PMU. The clock signals needed by the main charge pump are provided by the main oscillator. The MPPT block tunes the main charge pump topology and the frequency of the auxiliary and the main oscillators.

The MPPT block works in open-loop, continuous and two-dimensional mode, so it is always connected to the photodiode to determine different working regions according to the illumination. In other words, the voltage harvested by the photodiode defines the working regions. In the design phase, five different working regions were defined by simulation for the MPPT to cover the input voltage range of the photodiode, so four level detectors were designed to distinguish among the five working regions (WR1-WR5). The level detectors have a digital output which is high when V_{PD} is above the trigger voltage. Therefore, the MPPT method can be regarded as a lookup table defined in the design phase. Finally, a self-tuning reference current biased by V_{PD} adjusts the frequency of the auxiliary oscillator and it also performs a fine tuning of the frequency of the main oscillator independently of the working region, and thus independently of the charge pump topology. The MPPT block is

designed to meet the maximum PMU efficiency adjusting both the gain and the capacitance per stage of the main charge pump and the clock signals' frequency of both charge pumps.

The key contributions of this thesis in the field of solar micro-energy harvesting are reported in [78] and reproduced in Chapter 5, and can be summarized as:

1. An on-chip solar cell of 1 mm^2 and a PMU fabricated on the same substrate in standard 0.18 μm CMOS technology achieving a form factor of 1.575 mm^2.

2. A PMU starting up from a harvested power of 2.38 nW without any external kick off or control signal achieving a peak efficiency of 57% during normal operation.

3. A continuous and two-dimensional MPPT which works in open-loop mode, where the charge pump topology and the switching frequency are modified, handling an input power range from nW to μW.

More details about the energy harvesting system and its architecture can be found in Chapter 5.

And finally, the micro-energy harvesting system was presented as a live demo in the 2018 International Symposium on Circuits and Systems (ISCAS) [79]. To demonstrate the validity of the architecture, the system is illuminated with a lamp to power an off-chip multi-gate integrated circuit located on a breadboard unit and an oscilloscope is used to display the control and power supply signals. More details about the live demo with the micro-energy harvesting system can be found in Chapter 6.

To conclude, the micro-energy harvesting system was protected by the Spanish Patent and Trademark Office (OEPM) under the registration of the Topography of Semiconductor Products number T201730001(2) of December 11, 2017.

1.3. Thesis Outline

In the following chapters we provide the key publications that represent the main body of work for this thesis. In all these articles, the author of the thesis has been the main contributor. These articles have been either published in journals indexed in the Journal Citation Reports (JCR) or in high quality international conferences. The selection of publications has been made to delve into the main points mentioned in this introduction, and to have a more complete representation of the work carried out during this thesis. In Section 1.4, a full compendium of the journal and conference publications related to this thesis is presented.

In Chapter 2 we introduce a reliable model of the dynamic behavior of standard two-phase switched-capacitor DC-DC converters and their charge reusing versions with top and bottom parasitic capacitances in the SSL regime. The model is validated with both experimental results and circuit-level simulations achieving computation time savings of up to 10000×. Finally, it is used as a design tool to choose the best configuration in terms of speed and charge conversion efficiency for micro-energy harvesting constraints.

From the model presented in Chapter 2, we develop a simple and reproducible model of inverting charge pumps including the charge reusing technique in Chapter 3. The model is also validated with both experimental results and circuit-level simulations achieving computation time savings of up to 2000×.

In Chapter 4 a joint model which takes into account the dynamics of both the on-chip solar cell and the charge pump in the SSL regime is presented. The model is verified by circuit-level simulations showing high accuracy and achieving computation time savings of up to 1700×. The results presented demonstrate that failing to take into account the dynamics of the integrated micro-photovoltaic cell in the design of the capacitive DC-DC converter can lead to a sub-optimal design. Finally, the joint model is used to select the best charge pump configuration in terms of speed and charge efficiency for the particular situation of implantable devices.

A micro-energy harvesting system including a photodiode of 1 mm^2 and a PMU on the same substrate is presented in Chapter 5. The system is fabricated in standard 0.18 μm CMOS technology achieving a form factor of 1.575 mm^2. The PMU is able to start up from a harvested power of 2.38 nW without any external kick off or control signal. The PMU features a continuous and two-dimensional MPPT working in open-loop mode to handle a harvested power range from nW to μW.

In Chapter 6 the micro-energy harvesting system is presented as a live demo in the 2018 International Symposium on Circuits and Systems (ISCAS). The system illuminated by a lamp is used to power an off-chip multi-gate integrated circuit located on a breadboard unit. The control and power signals are displayed using an oscilloscope to demonstrate the operation of the system.

Then, the main conclusions and future work are drawn. And finally, Appendix A shows the details of the experimental setup to validate the charge pump model in Chapter 2 and Appendix B shows the different structures fabricated within the die with the micro-energy harvesting system presented in Chapter 5, as well as the experimental setup and measurements

of the structures which are not included in Chapter 5.

1.4. List of Publications

Following a list of publications derived from the work developed in this thesis is shown:
Articles in peer reviewed journals:

- E. Ferro, V. M. Brea, P. López, and D. Cabello, "Micro-Energy Harvesting System including a PMU and a Solar Cell on the same Substrate with Cold Start-Up from 2.38 nW and Input Power Range up to 10 μW using Continuous MPPT," *IEEE Transactions on Power Electronics*, Early Access.
  Impact factor (JCR 2017): 6.812. Q1.
  Category: ENGINEERING, ELECTRICAL & ELECTRONIC. Rank: **14/260**.

- E. Ferro, V. M. Brea, P. López, and D. Cabello, "Dynamic Model of Switched-Capacitor DC-DC Converters in the Slow-Switching Limit Including Charge Reusing," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5293–5311, July 2017.
  Impact factor (JCR 2017): 6.812. Q1.
  Category: ENGINEERING, ELECTRICAL & ELECTRONIC. Rank: **14/260**.

- E. Ferro, P. López, V. M. Brea, and D. Cabello, "Dynamic joint model of capacitive charge pumps and on-chip photovoltaic cells for CMOS micro-energy harvesting," *International Journal of Circuit Theory and Applications*, vol. 44, no. 10, pp. 1874–1894, 2016.
  Impact factor (JCR 2016): 1.571. Q3.
  Category: ENGINEERING, ELECTRICAL & ELECTRONIC. Rank: **145/262**.

Articles published in international conferences:

- T. A. Nevalainen, E. Ferro, V. M. Brea, P. López, and A. Paasio, "Low-Power Regulator for Micro Energy Harvesting Applications," in *2018 IEEE Nordic Circuits and Systems Conference (NorCAS)*, October 2018.

- E. Ferro, V. M. Brea, P. López, and D. Cabello, "Live Demonstration: Light Energy Harvesting System with an On-Chip Solar Cell and Cold Start-Up," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–1.

- E. Ferro, V. M. Brea, P. López, and D. Cabello, "Dynamic Model of On-Chip Inverting Capacitive Charge Pumps with Charge Reusing," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1626–1629.

- P. López, A. G. Loureiro, E. Ferro, V. M. Brea, and B. Rivas-Murias, "Study of the Thermoelectric Properties of Non-Typical Semiconductor Materials with Conventional CAD Tools," in *2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, April 2016, pp. 1–5.

- G. Capeáns, P. López, E. Ferro, A. G. Loureiro, D. Cabello, F. Rivadulla, and B. Rivas-Murias, "Design for Maximum Power Transfer Efficiency of Thermoelectric Generators using Mixed Mode Simulations," in *2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, April 2016, pp. 1–5.

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1.5. List of Inventions and Industrial Property Items

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CHAPTER 2

DYNAMIC MODEL OF SWITCHED-CAPACITOR DC–DC CONVERTERS IN THE SLOW-SWITCHING LIMIT INCLUDING CHARGE REUSING

E. Ferro, V. M. Brea, P. López, and D. Cabello, "Dynamic Model of Switched-Capacitor DC-DC Converters in the Slow-Switching Limit Including Charge Reusing," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5293–5311, July 2017

https://doi.org/10.1109/TPEL.2016.2607800

CHAPTER 3

DYNAMIC MODEL OF ON-CHIP INVERTING CAPACITIVE CHARGE PUMPS WITH CHARGE REUSING

E. Ferro, V. M. Brea, P. López, and D. Cabello, "Dynamic Model of On-Chip Inverting Capacitive Charge Pumps with Charge Reusing," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1626–1629

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CHAPTER 4

DYNAMIC JOINT MODEL OF CAPACITIVE CHARGE PUMPS AND ON-CHIP PHOTOVOLTAIC CELLS FOR CMOS MICRO-ENERGY HARVESTING

E. Ferro, P. López, V. M. Brea, and D. Cabello, "Dynamic joint model of capacitive charge pumps and on-chip photovoltaic cells for CMOS micro-energy harvesting," *International Journal of Circuit Theory and Applications*, vol. 44, no. 10, pp. 1874–1894, 2016

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CHAPTER 5

MICRO-ENERGY HARVESTING SYSTEM INCLUDING A PMU AND A SOLAR CELL ON THE SAME SUBSTRATE WITH COLD START-UP FROM 2.38 NW AND INPUT POWER RANGE UP TO 10 μW USING CONTINUOUS MPPT

E. Ferro, V. M. Brea, P. López, and D. Cabello, "Micro-Energy Harvesting System including a PMU and a Solar Cell on the same Substrate with Cold Start-Up from 2.38 nW and Input Power Range up to 10 μW using Continuous MPPT," *IEEE Transactions on Power Electronics*, Early Access

https://doi.org/10.1109/TPEL.2018.2877105

Chapter 6

Live Demonstration: Light Energy Harvesting System with an On-Chip Solar Cell and Cold Start-Up

E. Ferro, V. M. Brea, P. López, and D. Cabello, "Live Demonstration: Light Energy Harvesting System with an On-Chip Solar Cell and Cold Start-Up," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–1

https://doi.org/10.1109/ISCAS.2018.8351111

Conclusions and Future Work

The relevance of energy harvesting nowadays was introduced in this thesis. Light was selected as the energy source in this work because of its great power density. Furthermore, solar micro-energy harvesting allows to integrate sensing, processing and harvesting on the same silicon substrate, resulting in significant area, power and cost savings.

The work in this thesis ends up with experimental results of a micro-energy harvesting system as a proof-of-concept chip including a solar cell and a Power Management Unit (PMU) on the same substrate in standard 0.18 μm CMOS technology. The most relevant asset of our approach is that it is able to start-up from 2.38 nW and manage an input power range up to 10 μW without external or off-chip mechanisms to start up by using a continuous Maximum Power Point Tracking (MPPT), making it suitable for very low power applications in scenarios of difficult access like implantable devices. As our target is implantable devices, or in general low-power applications or systems, we aim at 1.1 V, so that our goal is to optimize energy efficiency, and thus power consumption, at 1.1 V. This means to optimize the power consumption of the charge pumps that rise up the voltage generated by on-chip photodiodes, below 0.3 V, up to the aforementioned 1.1 V.

We have started the way towards our final proof-of-concept chip in this thesis with a new model to study and help in the design procedure of capacitive DC-DC converters, also known as charge pumps. They are used to rise up the voltage provided by the on-chip solar cell up to a voltage level compatible with processing circuits in current standard CMOS technologies. Our model studies the dynamic behavior of standard two-phase switched-capacitor DC-DC converters and their charge reusing version with top and bottom parasitic capacitances in the Slow Switching Limit (SSL) regime. The model was illustrated for three capacitive DC-DC converter topologies: Dickson (LQP), Fibonacci (FQP) and exponential (EQP) charge pumps. The charge reusing approach reduces the charge consumed by LQP and both gain and

charge consumed for FQP and EQP. A methodology to design the capacitive DC-DC converter outside the SSL regime with a given error level with respect to circuit-level simulations in the switching frequency and switching transistor width parameter space was also addressed. The model was validated with experimental results and circuit-level simulations in the SSL region and it was compared with other models in the literature for LQP, FQP and EQP for both current and capacitive loads. The model also tackles dynamic loads, that combined with transient analysis permit to measure the output impedance of the DC-DC converter under study. Our model accounts for actual conditions that are not included in other models in the literature, featuring more reliable results. From the developed model, a web simulator that is up to 10000× faster than circuit-level simulators was built. As an example of applicability, the model was used as a design tool to choose the best configuration in terms of speed and charge conversion efficiency for micro-energy harvesting constraints.

From the model presented above, a new model of inverting charge pumps with and without the charge reusing technique was developed. The model also accounts for top and bottom parasitic capacitances. The model was validated with both experimental results and circuit-level simulations, and finally, the design procedure of an inverting Dickson charge pump for micro energy harvesting in standard 0.18 μm CMOS technology showing the effect of implementing the charge reusing technique was addressed.

Then, taken as starting point the dynamic model presented above, an accurate joint model for on-chip solar cells and two-phase switched-capacitor DC-DC converters in the SSL regime was presented. The model takes into account the dynamics of both the on-chip solar cell and the charge pump. The model also includes the top and bottom parasitic capacitances of the converter. It was verified by circuit-level simulations showing high accuracy and achieving computation time savings of up to 1700×. The results presented in this thesis demonstrate that failing to take into account the dynamics of the integrated micro-photovoltaic cell in the design of the capacitive DC-DC converter can lead to a sub-optimal design. As an application example, the joint model was used to select the best configuration in terms of speed and charge efficiency for the particular situation of implantable devices taking into account area or time response constraints.

From the models introduced above, a charge pump plus other essential blocks were designed to be integrated in a Power Management Unit (PMU) powered by an on-chip solar cell. Therefore, a new system for micro-energy harvesting including a photodiode and a PMU on the same substrate was designed and fabricated in standard 0.18 μm CMOS technology

achieving a form factor of 1.575 mm^2. The 1 mm^2 photodiode is the only power source of the system. The PMU includes a continuous and two-dimensional Maximum Power Point Tracking (MPPT) to manage an input power range from nW to μW. Our MPPT technique follows a look-up table methodology, whereby a given frequency, a given DC-DC converter gain and certain capacitor sizes are set by a digital control according to five different working regions defined by the voltage provided by the micro-solar cell. Thus, our approach is an open-loop system, which brings about low power as the main benefit. This can be clearly seen when compared to previous state-of-the-art work, as our approach features the lowest input power, namely 2.38 nW, to start-up the system without external kick off reported in the literature.

Future Work

In the short-term future, there is a follow-up of our proof-of-concept energy harvesting chip under fabrication, manufactured with the same technology, this is, standard 0.18 μm CMOS technology. This chip addresses three concerns raised up during the characterization of our first proof-of-concept chip, namely, unexpected drops of energy efficiency, sensitivity to the infrared radiation and the lack of output voltage regulation. The first one is addressed with a more elaborate joint model of photodiode or micro-solar cell and PMU, by including experimental data from our first chip. The second one is tackled blocking the infrared radiation by using layout techniques as explained in Appendix B. The last one is addressed with an on-chip voltage regulator. It consists of an on-chip 1.1 V voltage generator and a very-low power consumption clocked comparator to disconnect the main oscillator through power gating when the output voltage of the main charge pump reaches 1.1 V. Experimental results of this new chip will be available soon.

In the medium- and long-term future, overvoltage and undervoltage protection circuits could be included in order to add a very small battery to the micro-energy harvesting system. Also, a better voltage regulator including several reference voltages will be useful to power each sensing or processing block of the chip with the adequate voltage, avoiding high power consumptions. Finally, in a more long-term future, the micro-energy harvesting system, particularly the PMU, could be extended to deal with mW of input power, useful in applications like Internet of Things (IoT).

APPENDIX A

EXPERIMENTAL SETUP TO VALIDATE THE CHARGE PUMP MODEL IN CHAPTER 2

The charge pump model presented in Chapter 2 has been compared to other models in the literature and validated through experimental results. In this Appendix details about the experimental procedure to validate the model are drawn.

A Printed Circuit Board (PCB) with different topologies of capacitive DC-DC converters was designed. In this case, we included Dickson, Fibonacci and exponential charge pumps of 8× gain (LQP8×, FQP8×, EQP8×) with and without the charge reusing technique. The PCB was designed to use through-hole capacitors to enable the possibility of changing the total capacitance or to try different capacitance values for each stage of the charge pumps. To reproduce the actual behavior of on-chip capacitors, tantalum capacitors are more appropriate because of their low leakage currents. Regarding the switches, a TS5A23166 circuit was chosen due to its low on-resistance ($R_{on} = 0.9\Omega$).

Figure A.1 shows the fabricated PCB. It was designed using the software EAGLE from Autodesk. The PCB of 2 layers is made of 1.6 mm thickness FR4 material with 35 μm thickness of copper tracks. In Figure A.1 we can see the different capacitors, the TS5A23166 circuits as used switches and the connectors to externally control and measure the charge pumps.

The entire experimental setup is shown in Figure A.2. It consists of a power supply, the PCB with the different charge pump topologies, a Data Acquisition (DAQ) board and a computer with LabVIEW from National Instruments. The power supply is used as the input

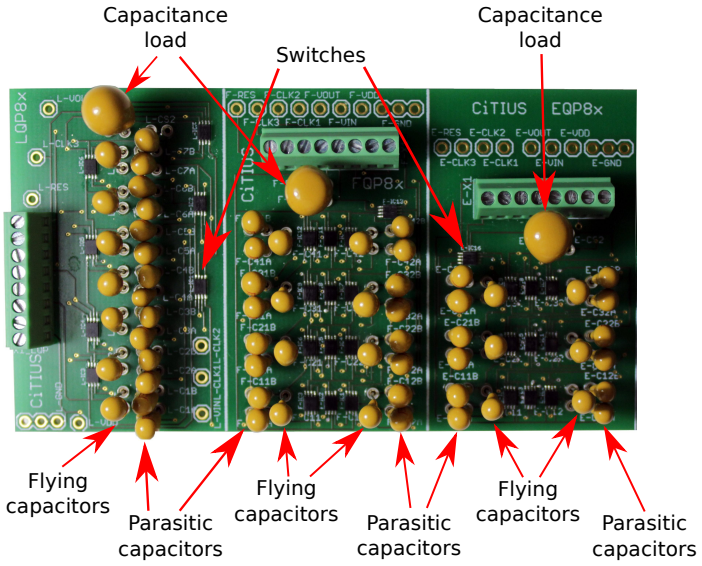


Figure A.1: PCB with DC-DC converters LQP8×, FQP8× and EQP8× with and without charge reusing.

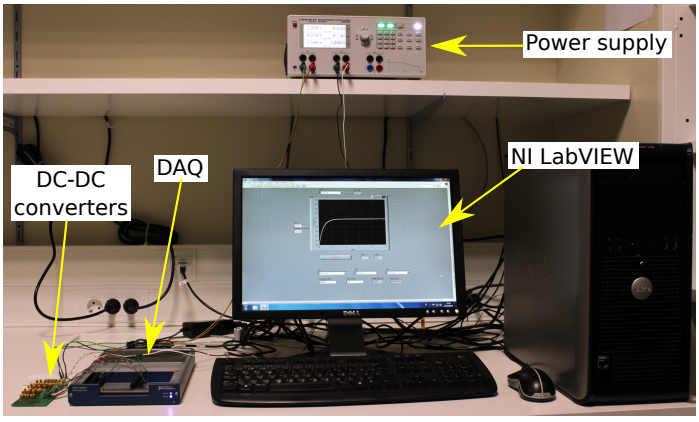


Figure A.2: Experimental setup for the validation of the model in Chapter 2.

power for the charge pumps and to power the TS5A23166 circuits. The DAQ board controls and measures the charge pumps and LabVIEW is used to program the DAQ and to display and save the results.

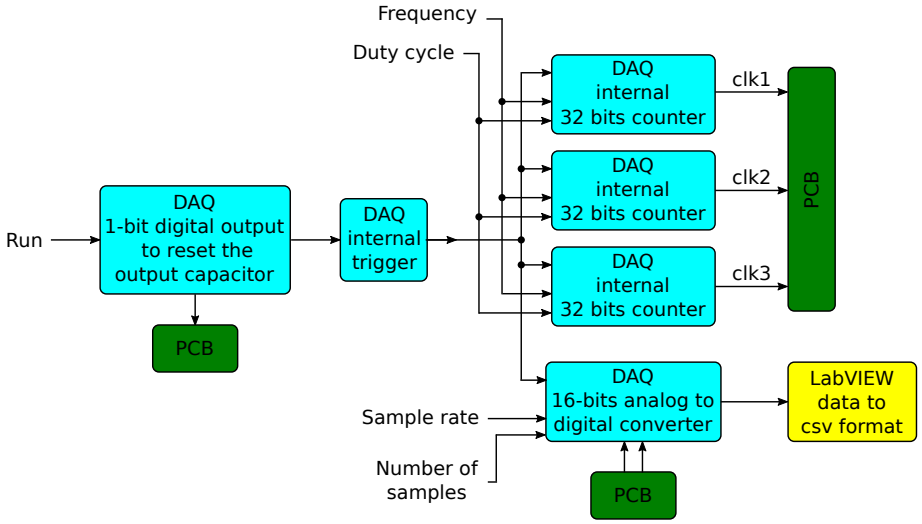


Figure A.3: Flow diagram of the measurement procedure using LabVIEW to control de DAQ board.

The DAQ model chosen for this experimental setup is the USB-6341 from National Instruments. It includes a 16-bits analog to digital converter (ADC) of 500 kS/s for 16 single ended channels, 2 analog output channels, 24 digital input/output digital channels, 4 counters of 32 bits and a channel with a frequency generator by means of a PLL. We use LabVIEW to directly control the different hardware parts of the DAQ board.

In Figure A.3 a flow diagram of the measurement procedure is shown. First, we need to set the frequency and duty cycle of the clock signals for the charge pump. Also, we need to set the sample rate and number of samples of the DAQ's ADC. After that, a digital output of the DAQ board turns on a switch to reset the output capacitor of the charge pump. Then, a DAQ internal trigger activates 3 counters and the ADC at the same time. The 3 counters generate the two non-overlapping signals $clk1$ and $clk2$, and the clock signal, $clk3$, for implementing the charge reusing technique. If the charge reusing is not needed, $clk3$ is set to 0 V. The ADC reads the voltage at the output of the charge pump. The ADC also reads the voltage across a 1.9 Ω resistor placed in the input of the charge pump in order to measure the current entering the DC-DC converter. This resistor does not affect the charge pump behavior because the measurements are made in the SSL regime. Finally, the data are plotted and saved in csv format.

APPENDIX B

PROOF-OF-CONCEPT MICRO-ENERGY HARVESTING SYSTEM TEST

The micro-energy harvesting system presented in Chapter 5 was fabricated in standard 0.18 μm CMOS technology. In Section B.1 the design procedure of the system is introduced. Also, details about the different fabricated structures within our proof-of-concept chip are shown in Section B.2. The experimental setup is explained in Section B.3, and finally, additional experimental results are shown in Section B.4.

B.1. Design Constraints and Methodology

One of the goals of this thesis is to design a micro-energy harvesting system in standard 0.18 μm CMOS technology including a photodiode and a Power Management Unit (PMU) for low power applications. The architecture developed for this purpose is general and it can be adapted for different applications, like Internet of Things (IoT) or wearable computing. However, for the sake of clarity, we have illustrated the design of the micro-energy harvesting system for the constraints of implantable devices. Particularly, the target of the system is to power the circuitry needed to measure the intraocular eye pressure including a microelectromechanical systems (MEMS) sensor and a wireless communication circuit.

The area restrictions in the eye have forced us to choose the area of the photodiode to be 1 mm^2. This limits the energy harvested by the photodiode and therefore, the energy available to power the system. Estimations of the power generated by the photodiode of 1 mm^2 were

made by running device-level simulations with ATLAS from Silvaco®. The estimated doping profiles for the simulations are supplied by the technology provider. Structures with different layers and finger pitches were simulated to choose the structure which generates more power for the same illumination. The chosen structure is a p^+ over P-Well in NWell with a separation of 1 μm between fingers, which generates an estimated power of μW at 100 klx.

As the photodiode generates a voltage below 0.5 V, a DC-DC converter is needed to rise up this voltage up to the target voltage of 1.1 V, which is more appropriate for low power applications than the nominal voltage of 1.8 V of the chosen technology. We have chosen a charge pump as the best option for this purpose in the case of implantable devices, and in order to help in the design process of capacitive DC-DC converters driven by two non-overlapping clock signals, we have developed a new model. As we have introduced in Chapter 4, this model takes into account the dynamics of both the photodiode and the charge pump. Therefore, taking as starting point the device-level simulations of the photodiode for different illuminations, this new model implemented in Matlab® have helped us to choose the gain, capacitance per stage and frequency of the clock signals for the main charge pump, optimizing the relation among power, area and speed for those different illuminations.

Regarding the auxiliary charge pump, it was designed with the help of the new model presented in Chapter 2, which analyzes the dynamic behavior of two-phase switched-capacitor DC- DC converters in the slow-switching limit regime. The oscillators were designed following the equations presented in the literature in order to match the frequency requirements obtained with the joint model and the level shifters were designed following the literature to reach very low power consumption [84, 85].

Finally, the Maximum Power Point Tracking (MPPT) block permits to transfer the maximum power from the photodiode to the load for any illumination. This block was designed to follow the requirements set by the charge pump models. However, as all the blocks are related to each other due to the fact that they are powered by the same photodiode and therefore, the consumption of one single block implies a decrease in the voltage generated by the photodiode, circuit level simulations with CAD tools of the whole PMU were performed for a fine adjustment of all the charge pump parameters, as for example, the capacitance per stage or the clock frequencies. Also, most transistors work in the subthreshold region for which process variations have high influence, so to finish the design of the PMU, exhaustive Montecarlo simulations were run.

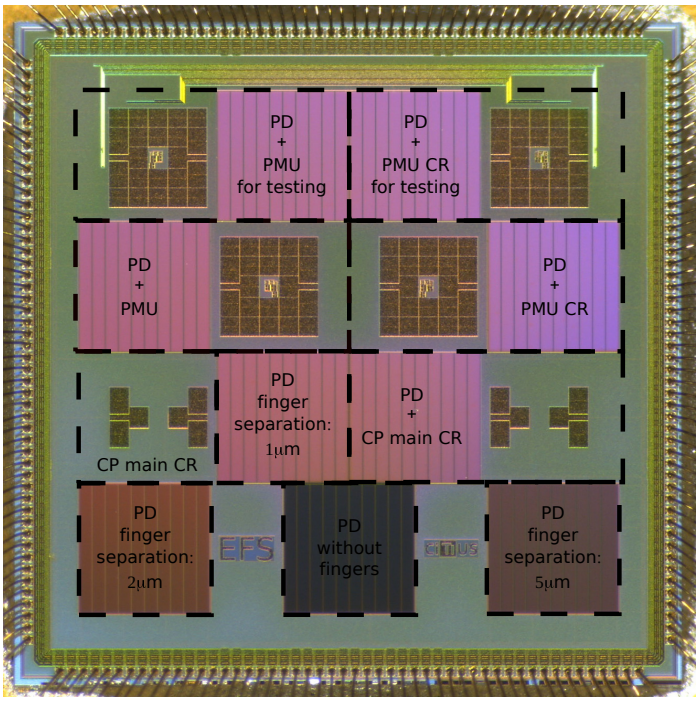


Figure B.1: Die photograph of the fabricated chip.

B.2. Chip Floorplan

Figure B.1 shows a die photograph of the fabricated chip. The layout distribution is the adequate to avoid structural issues since the photodiodes do not comply with the minimum metal density design rules. On the bottom-half of the figure, labeled *PD*, we can see four 1 mm^2 p^+ over P-Well in NWell photodiodes with different separation between fingers. On the half-left and labeled *PD+PMU*, we can see the system proposed in Chapter 5, where only the output of the main charge pump is accessible. On the top-left and labeled *PMU+PD for testing*, we can see the same system but with access to 44 different internal nodes for testing. On the right of the figure we can see the same structures as on the left side, but with the main charge pump with the charge reusing technique (*CR*). We can also see an isolated charge pump with the same configuration as in the above systems labeled *CP main CR* and another isolated charge pump but with a photodiode as input labeled *PD+CP main CR*.

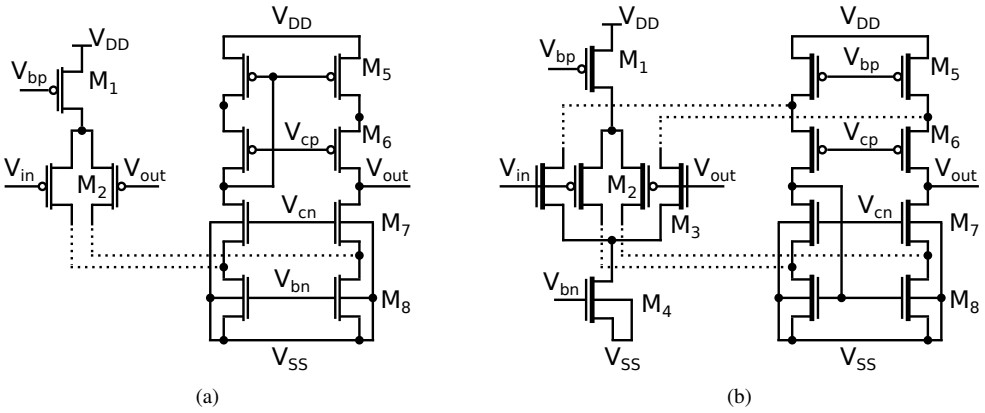


Figure B.2: Schematics of the buffers to measure the internal nodes of the micro-energy harvesting systems with a 0.5 V input voltage range buffer in (a) and a 2.5 V input voltage range buffer in (b).

The number of pads of the die is 200, so the die is encapsulated in a CPGA 208 pins package. Of these, 33 pads are for the ground, 1.8 V and 3.3 V power supply voltages. 26 are input digital pads to control the isolated charge pumps and the remaining pads are analog pads with electrostatic discharge (ESD) protection for the inputs and outputs of the two isolated charge pumps, for the outputs of the micro-energy harvesting systems with and without charge reusing, to access to the internal nodes of the systems for testing, and for the bias voltage and voltage supply of on-chip buffers.

On-chip buffers in the PMUs for testing are used to deal with the large fan-out from the pads and the measuring equipment. Despite performing a careful design, these buffers also modify the nodes of interest due to their input capacitance, adding inaccuracies during measurement. Still, behavioral studies can be performed. For example, the response of the level detectors of the MPPT block shown in Figure 5.16 in Chapter 5 is measured through these buffers. Figure B.2 shows the two different buffer topologies both designed as folded-cascode opamps used to drive the pads in order to measure the internal nodes of the micro-energy harvesting system. Each topology corresponds to two different input voltage ranges: $[0-0.5]$ V and $[0-2.5]$ V. The former are used to measure signals powered directly by the photodiode, while the latter are used to measure signals powered by the auxiliary DC-DC converter. All the NMOS transistors of the buffers are fabricated over P-Well to reach $V_{SS} < 0$ in order to increase the dynamic input/output voltage ranges down close to ground, allowing

Table B.1: Size of the transistors of the on-chip buffers used to measure the internal nodes of the micro-energy harvesting systems

	slow 0.5 V buffer		fast 0.5 V buffer		slow 2.5 V buffer		fast 2.5 V buffer	
	width (μm)	length (μm)	width (μm)	length (μm)	width (μm)	length (μm)	width (μm)	length (μm)
M1	5.5	2	17.04	2	9.12	3	12	2
M2	18	3	45.04	1	13.98	2	22	1
M3	-	-	-	-	13.98	2	22	1
M4	-	-	-	-	9.04	3	12	2
M5	3	2.2	70	1.5	25	3	70	1.5
M6	3.2	2.2	30	1.5	25.04	3.5	50	1.5
M7	10	3	49.98	1.5	25.04	3	60	1.5
M8	6	3.75	95	1.5	18	3.25	95	1.5

Table B.2: Specifications of the on-chip buffers without load

	slow 0.5 V buffer	fast 0.5 V buffer	slow 2.5 V buffer	fast 2.5 V buffer
V_{SS} (V)	-0.5	-0.5	-0.2	-0.2
V_{DD} (V)	1.3	1.3	3.1	3.1
supply current (μA)	10.27	113.16	22.08	105.68
open-loop gain (dB)	50.55	43.70	56.20	40.83
gain error (%)	0.23	0.16	0.32	1.97
offset (mV)	1.53	2.81	3.95	14.34
linearity error (%)	0.0064	0.035	0.44	1.13
cut-off frequency (kHz)	260.70	954.63	196.14	946.07
rise time (μs)	0.019	0.0058	0.054	0.043
fall time (μs)	0.023	0.0054	0.069	0.055

Table B.3: Specifications of the on-chip buffers with $C_L = 20$ pF and $R_L = 1$ MΩ

	slow 0.5 V buffer	fast 0.5 V buffer	slow 2.5 V buffer	fast 2.5 V buffer
V_{SS} (V)	-0.5	-0.5	-0.2	-0.2
V_{DD} (V)	1.3	1.3	3.1	3.1
supply current (μA)	10.51	113.42	22.07	105.68
open-loop gain (dB)	28.38	40.54	27.83	29.92
gain error (%)	3.98	0.69	3.17	2.93
offset (mV)	1.88	2.99	1.47	13.05
linearity error (%)	0.26	0.11	1.57	1.12
cut-off frequency (kHz)	8.50	18.36	11.87	16.88
rise time (μs)	2.65	0.27	7.49	4.69
fall time (μs)	2.50	0.21	8.03	4.99

more accurate measurements of voltages close to zero. Two different buffers for each voltage range are designed: slow and fast buffers. Table B.1 summarizes the size of the transistors of every designed buffer.

The buffer topology to measure a voltage range from 0 to 0.5 V is shown in Figure B.2(a). All the transistors of this topology have regular threshold voltage. Figure B.2(b) shows the

buffer topology to measure a voltage range from 0 to 2.5 V. All the transistors of this topology have high threshold voltage to deal with the high input voltage range. Table B.2 and Table B.3 show the characteristics of the on-chip buffers without load and with both capacitive and resistive load, respectively. As Table B.2 shows, the slow buffers were designed to have higher open-loop gain and smaller offset and linearity error than the fast ones. Nevertheless, the fast buffers have higher open loop-gain than the slow ones in the situation with load, although the offset is still higher for the fast buffers. That is because the buffers designed as folded-cascode opamps or Operational Transconductance Amplifiers (OTAs) are more appropriate to drive pure capacitive loads [86]. However, most laboratory instruments have such a high input impedance that they can be considered capacitive loads. Also, the slow buffers have low supply current to deal with slow input signals and to avoid high power consumption through the chip as 89 buffers are used to access to internal nodes, and the self-heating effects plus the heating of a lamp could have negative effects in the chip as well.

In conclusion, the on-chip buffers were designed to take measurements of the internal nodes of the micro-energy harvesting systems, however, the input capacitance of the buffers and their own design errors avoid accurate measurements, so only the behavior of the internal signals can be studied.

B.3. Experimental Setup

Figure B.3 shows the Printed Circuit Board (PCB) designed to have access to all the connections of the fabricated chip and to power the pads with ESD protection. The PCB has voltage regulators model TPS73701 to power the pads at 1.8 V and 3.3 V and an inverter charge pump model MAX889 to generate -3.3 V. The bias voltages for the on-chip buffers for testing are generated with voltage dividers between 3.3 V and -3.3 V. Also, level shifters model SN74LV4T125 with an output voltage level of 3.3 V needed for the digital input pads are used to adapt the digital signals generated externally to control the isolated charge pumps. The power supply for all the circuits mentioned above is supplied through an USB connector. Finally, the supply voltages for the on-chip buffers are generated with an external power supply in order to avoid noisy power signals from the inverter charge pump.

An LED lamp, model 5W CorePro LEDspot LV of Philips, is used to illuminate the on-chip solar cell as it is shown in Figure B.4. To establish the illumination received by the on-chip solar cell, both the voltage of the lamp and the distance to the chip can be controlled.

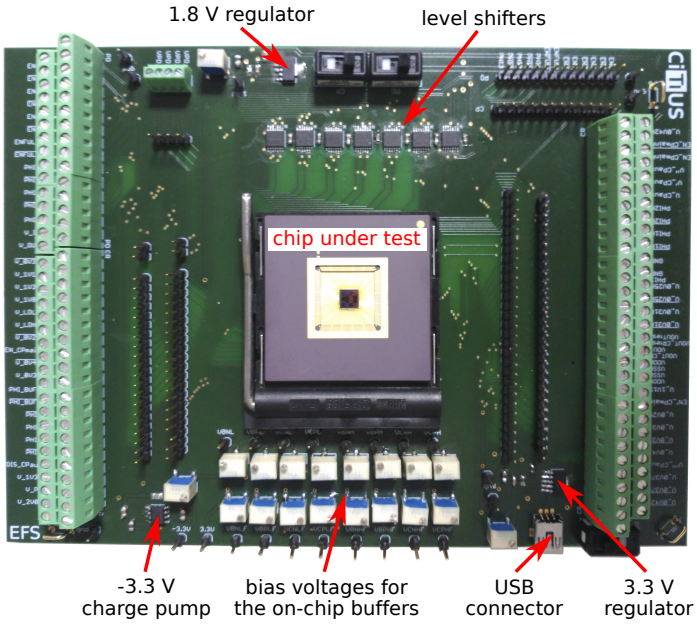


Figure B.3: PCB for the die testing.

Figure B.4: Experimental setup of the chip under test.

So, for example, for high illumination (100 klx), we power the lamp with 12 V and decrease the distance between the chip and the lamp to a few centimeters. A digital lux meter (TES 1332) is used to measure the illumination that reaches the chip. Figure B.4 also shows an oscilloscope (Tektronix MDO4034C) to visualize the output and the control signals of the

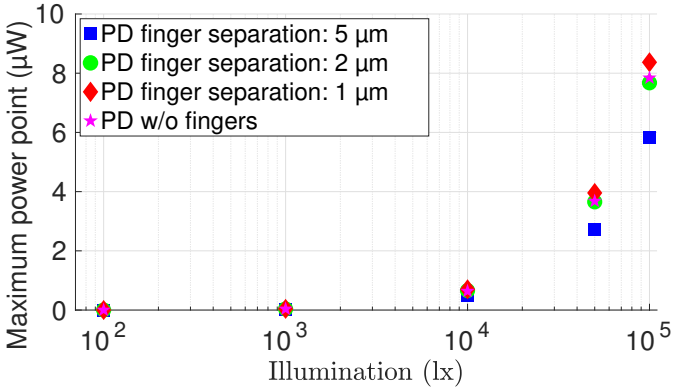


Figure B.5: Comparison of the power generated by the different photodiode configurations for different illuminations.

chip. One source meter unit (2400 Keithley SMU) is used to measure the output power of the micro-energy harvesting systems and another source meter unit (2450 Keithley SMU) is used to measure the P-V curves of the photodiodes. As in the case of the validation of our model of DC-DC converters addressed in Appendix A, a DAQ and LabVIEW are used to control the isolated charge pumps.

B.4. Additional Experimental Results

The experimental results related to the micro-energy harvesting system without the charge reusing technique are detailed in Chapter 5. Results for the other structures on this chip are commented in this Section. In Section B.4.1 the different photodiode configurations are explained. Isolated charge pumps are tested in Section B.4.2 and the PMU with the main charge pump implementing the charge reusing technique is introduced in Section B.4.3. Finally, the effect of the infrared radiation on the PMU is commented in Section B.4.4

B.4.1. Photodiode Configurations

In order to increase the efficiency per area of a photodiode, four different photodiodes of 1 mm^2 with different separation between fingers were designed to be included on the chip as Figure B.1 shows. This allows us to measure which configuration generates more power for

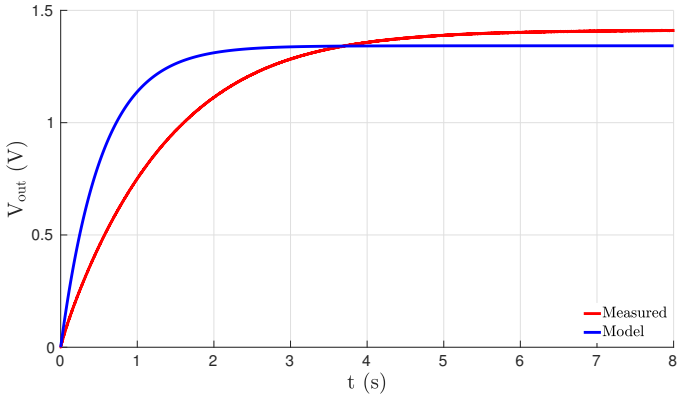


Figure B.6: Comparison of the model and the experimental results of the isolated charge pump configured with 7× gain.

the same illumination. Figure B.5 depicts the maximum power points for different illuminations. The photodiode with a separation of 1 µm between fingers generates more power than the other ones with other separation or without fingers for the same illumination. We hypothesize that this behavior is because the PWell depth is approximately 1 µm. This photodiode configuration is used to design the photodiodes which power the micro-energy harvesting systems and the isolated charge pump.

B.4.2. Isolated Charge Pump

An isolated charge pump labeled *CP main CR* in Figure B.1 similar to the main charge pump of the PMU with charge reusing is also included on the chip to experimentally verify the charge pump model introduced in Chapter 2. We prepare an experimental setup to test the isolated charge pump similar to the one in Appendix A, using the same DAQ and LabVIEW. We set the sample rate of the analog to digital converter of the DAQ at 500 kS/s to take 4,000,000 samples. We also set the clock frequencies at 10 kHz with a duty cycle of 0.47, $V_{in} = 0.2$ V and $C_{out} = 100$ nF. We choose the configuration of the isolated charge pump to have 7× gain and the charge reusing technique off. We suppose 10% and 5% of the flying capacitor values for bottom and top parasitic capacitances for our model presented in Chapter 2, respectively. Figure B.6 compares the experimental results with the results obtained using our model. The results show some differences in both gain and rising time. Our guess is that the

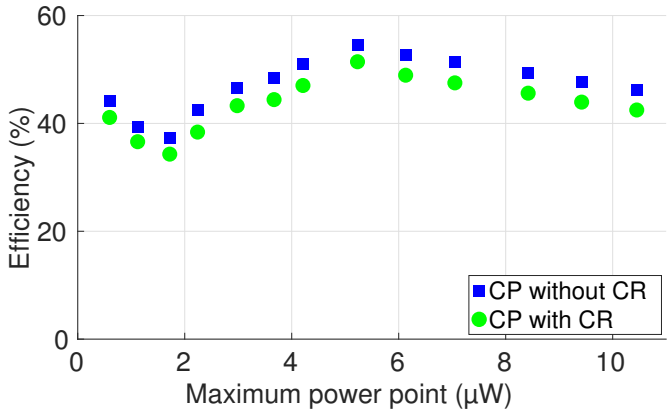
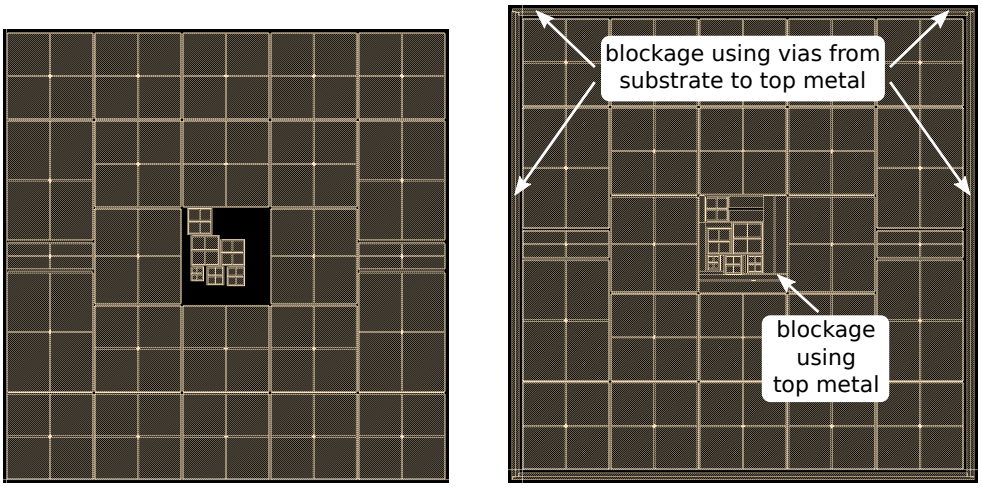


Figure B.7: Comparison of the efficiency of the micro-energy harvesting system with and without the charge reusing technique.

estimated values for the parasitic capacitances for our model differ from the real ones and to a lesser extent, the transistors used as switches to configure the gain and the capacitance per stage of the charge pump can present some current leakage and parasitic capacitances, being difficult to include them in our model. The same conclusion can be extended to the isolated charge pump with a photodiode as input included on the chip (labeled *PD+CP main CR* in Figure B.1) to validate the joint model in Chapter 4.

B.4.3. Charge Reusing Technique on the PMU

A micro-energy harvesting system with the main charge pump implementing the charge reusing technique is also included on the chip in order to test the efficiency of the whole PMU implementing this technique. The charge reusing technique, as explained in Chapter 2, leads to higher gain and better charge or energy efficiency by adding a clock signal and some switches linking the bottom parasitic capacitances of the charge pumps. To include this technique in the PMU implies to modify the main oscillator to generate a third clock signal and it also implies to change the main charge pump. However, the PMU area is not affected by these changes. The PMU with charge reusing is measured following the procedure presented in Chapter 5. Figure B.7 compares the efficiency of the micro-energy harvesting systems with and without charge reusing for high illumination, where the main charge pump is configured with high capacitance per stage and high clock frequency. We can see that, contrary to our



(a) (b)

Figure B.8: Comparison of the layout of the PMU with and without infrared blockage, with the fabricated PMU in (a) and the PMU with infrared blockage of the ongoing chip in (b).

expectations from the simulations with the model introduced in Chapter 2, the charge reusing technique decreases the efficiency of the system. We hypothesize that the actual parasitic capacitances are smaller than expected, being the charge required to generate the third non-overlapping clock signal for the charge reusing technique larger than the charge saved with this technique.

B.4.4. Infrared Effects on the PMU

To perform all the measurements introduced above we have used an LED lamp as shown in Figure B.4. The reason under this choice is that the infrared radiation affects the level detectors changing their trigger voltages. Our guess is that this type of radiation generates charges in the N-Well of each level detector affecting their trigger voltages. We have used an infrared filter to get the PMU working properly under solar illumination, so one solution to solve this problem could be to use a post-fabrication process to add an infrared filter over the chip. Other solution could be to block the infrared radiation by using layout techniques as in Figure B.8(b). This solution was adopted in a follow-up chip of our current proof-of-concept chip. Our solution was to cover the PMU with top metal and to add vias connecting the

substrate with the top metal around the PMU to prevent the infrared radiation from reaching the level detectors by means of reflections between metal layers.

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List of Figures

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